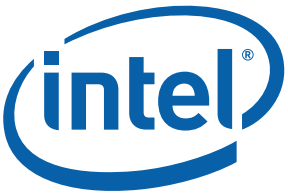

Intel® IXP43X Product Line of Network Processors

Datasheet

Product Features

This document describes the features of the Intel® IXP43X Product Line of Network Processors. Refer to Section 1.0 for a complete list of all the features. Some of these features require enabling software supplied by Intel. Refer to the *Intel® IXP400 Software Programmer's Guide* for information on features that are currently enabled.

These features do *not* require enabling software

- Intel XScale® Processor — Up to 667 MHz
- PCI v. 2.2 32-bit 33 MHz (Host/ Option)
- Two USB v2.0 Host Controller
- DDRI-266 MHz/DDRII-400MHz SDRAM Interface
- Slave Interface Expansion bus
- One UART
- Internal Bus Performance Monitoring Unit
- 16 GPIO
- Four Internal Timers
- Synchronous Serial Protocol (SSP) Port
- I^2C Interface
- Packaging
  - — 460-Pin PBGA
  - — Commercial Temperature
  - — Lead-Free Support

These features require enabling software. For information on features that are currently enabled see the *Intel® IXP400 Software Programmer's Guide*.

- Encryption/Authentication (AES/ AES-CCM/3DES/DES/SHA-1/SHA-256/ SHA-384/SHA-512/MD-5)
- One High-Speed Serial Interface
- Two Network Processor Engines
- Up to two MII Interfaces
- One UTOPIA Level 2 Interface

Typical Applications

- SOHO-Small Business/ Residential Modular Router
- Wireless Gateway (802.11a/b/g)
- Network-Attached Storage
- Wired/Wireless RFID Readers
- Digital Media Adapter
- VoIP Router
- Video Phone
- Security Gateway/Router
- Network Printers
- Wireless Media Gateway
- IP Set Top box

Document Number: 316842; Revision: 002US
August 2007

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Revision History

Date	Revision	Description
August 2007	002	Section 1.1, and Section 1.2: • Added extended temperature support • Removed references to 266 MHz clock speed on Intel® IXP43X Product Line of Network Processors Section 3.0: • Figure 1, Figure 2, and Figure 5: Removed 266 MHz clock speed • Figure 3, and Figure 4: Modified 266 MHz clock speed to 400 MHz clock speed Section 5.0: • Table 27: Updated Estimated Power Value • Table 29: Removed 266 MHz for V_{CC} Section 5.9: Table 71: • 1. Added DDR2 Power Dissipation value and modified the Typical Power Dissipation values • 2. Removed Intel® IXP43X Product Line of Network Processors - 266 MHz
April 2007	001	Initial release

§ §

1.0 Features of the Intel® IXP43X Product Line of Network Processors

1.1 Product Line Features

Table 1 on page 12 describes the features that apply to the Intel® IXP43X Product Line of Network Processors.

This section describes all the features of this silicon. Some of the features require software delivered by Intel and those features may not be enabled with current software releases.

The features that require software are covered in this document. Refer to the *Intel® IXP400 Software Programmer's Guide* for information on features that are currently enabled.

- Intel XScale® Processor (compliant with Intel® StrongARM* architecture)
  - — High-performance processor based on Intel XScale® Technology
  - — Seven/eight-stage Intel® Super-Pipelined RISC Technology
  - — Memory management unit (MMU)
    - 32-entry, data memory management unit
    - 32-entry, instruction memory management unit (MMU)
    - 32-KByte, 32-way, set associative instruction cache
    - 32-KByte, 32-way, set associative data cache
    - 2-KByte, two-way, set associative mini-data cache
    - 128-entry, branch target buffer
    - Eight-entry write buffer
    - Four-entry fill and pend buffers
  - — Clock speeds:
    - 400 MHz
    - 533 MHz
    - 667 MHz
  - — Intel® StrongARM* Version 5TE Compliant
  - — Intel® Media Processing Technology
    Multiply-accumulate coprocessor
  - — Debug unit
    Accessible through JTAG port
- PCI interface
  - — 32-bit interface
  - — Selectable clock
    - 33-MHz clock output produced by GPIO15. **Note 1**
    - 1- to 33-MHz clock input
  - — *PCI Local Bus Specification*, Revision 2.2 compatible
  - — PCI arbiter supporting up to four external PCI devices (four REQ/GNT pairs)
  - — Host/option capable
  - — Master/target capable

  - Two DMA channels
- Two USB v2.0 host controller
  - Low, full and high-speed capable
  - Embedded transceiver
  - EHCI Compliant
  - UTMI+ Level 2 compliant
- DDRI-266 or DDRII-400 interface
  - Internally multi-ported memory controller unit (Three internal ports)
  - 16/32-bit data
  - 14-bit address
  - 133.32 MHz for DDRI and 200 MHz for DDRII-400
  - Supports 128/256/512/1,024-Mbit technologies for DDRI-266
  - Supports 256/512-Mbit technologies for DDRII-400
  - Unbuffered DDRI and DDRII SDRAM support only
  - Up to eight open pages simultaneously maintained
  - Support for 16 MB, minimum for DDRI-266, 32 MB minimum for DDRII-400; 1 GB, maximum for DDRI-266, 512 MBs maximum for DDRII-400
  - User enabled, single bit error correction/multi-bit error detection ECC support
  - Supports two physical banks of DDR SDRAM in the form of discrete chips only
- Expansion interface
  - 24-bit address
  - 16-bit data
  - Four programmable outbound chip selects
  - Outbound transfer support
    - Supports Intel/ Motorola* microprocessor bus cycles
    - Multiplexed-style bus cycles
    - Non-multiplex bus cycles
    - 16 bit Synchronous flash support
    - Up to 80-MHz operation at 25 pF load
- One UART interface
  - 1,200 Baud to 921 Kbaud
  - 16550 compliant
  - 64-byte Tx and Rx FIFOs
  - CTS and RTS modem-control signals
- Synchronous serial port interface
  - Master mode only
  - Serial Peripheral Interface (SPI) of Motorola*
  - National's Microwire*
  - Synchronous Serial Protocol (SSP) of Texas Instruments*
- Internal bus performance monitoring unit (IBPMU)
  - Seven 27-bit event counters

  - — Monitoring of internal-bus occurrences and duration events
- 16 GPIOs
- Four internal timers
  - — Watchdog timer
  - — 2 General-Purpose timers
  - — Timestamp timer
- Clock
  - — 33.33 MHz Oscillator
  - — Spread-Spectrum Support
- Packaging
  - — 460-pin PBGA
  - — 31 mm by 31 mm
  - — Commercial temperature (0° to 70° C)
  - — Extended temperature (-40° to 85° C)
  - — Lead free support

The remaining product line features listed below require software in order to be functional. To determine whether a feature is enabled or not, refer to the *Intel® IXP400 Software Programmer's Guide*.

- Two network processor engines (NPE A and NPE C)
  Used to off load typical Layer-2 networking functions such as:
  - — Ethernet filtering
  - — ATM SARing
  - — HDLC
  - — Security acceleration (AES/DES/3DES/SHA/MD-5)
- Network interfaces that can be configured in the following manner:
  - — Two MII interfaces
  - — One MII interface + 1 UTOPIA Level 2 interface
- MII interfaces are:
  - — 802.3 MII interfaces
  - — Single MDIO interface to control the MII interfaces
- UTOPIA Level 2 Interface is:
  - — Eight-bit interface
  - — Up to 33-MHz clock speed
  - — Five transmit and five receive address lines
- Encryption/Authentication
  - — DES
  - — Triple-DES (3DES)
  - — AES 128-bit, 192-bit, and 256-bit
  - — Single-pass AES-CCM
  - — SHA-1, SHA-256, SHA-384, SHA-512
  - — MD-5

- One high-speed, serial interface
  - — Six-wire
  - — Supports speeds up to 8.192 MHz
  - — Supports connection to T1/E1 framers
  - — Supports connection to CODEC/SLICs
  - — Four HDLC channels
  - — Clock source provided from an external source or internal HSS clock divider

Note:

1. The Intel® IXP42X product line of network processors and Intel® IXP46X product line of network processors support up to 66 MHz PCI operations while the Intel® IXP43X Product Line supports up to 33 MHz PCI operations.

1.2 Model Specific Features

Table 1. Intel® IXP43X Product Line of Network Processors Features

Features	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
Processor Speed (MHz)	400 / 533 / 667	533	400	400	400 / 533 / 667
GPIO	X	X	X	X	X
UART 0	X	X	X	X	X
HSS 0 (NPE-A)†	X	X		X	
UTOPIA Level 2 (NPE A)†	X			X	
MII (NPE-A)†	X	X	X		X
MII (NPE-C)†	X††	X	X	X	X
USB v. 2.0 Hosts	X	X	X	X	X
PCI	32-bit, up to 33-MHz	32-bit, up to 33-MHz	32-bit, up to 33-MHz	32-bit, up to 33-MHz	32-bit, up to 33-MHz
Expansion Bus	16-bit, up to 80-MHz	16-bit, up to 80-MHz	16-bit, up to 80-MHz	16-bit, up to 80-MHz	16-bit, up to 80-MHz
DDRI-266 or DDRII-400 DRAM	16/32-bit	16/32-bit	16/32-bit	16/32-bit	16/32-bit
AES/AES-CCM/DES / 3DES†	X		X		
SHA / MD-5†	X		X		
Multi-Channel HDLC†	X	X		X	
SSP	X	X	X	X	X
Commercial Temperature	X	X	X	X	X
Extended Temperature	X				X

† These features require Intel supplied software to be operational. Refer to the *Intel® IXP400 Software Programmer's Guide* to determine whether a feature is enabled or not.

†† Only 1 10/100 MAC is available if the UTOPIA interface is used.

2.0 About This Document

This document provides the following:

- Functional overview of the Intel® IXP43X Product Line of Network Processors
- Mechanical data (package signal locations and simulated thermal characteristics)
- Targeted electrical specifications
- Bus functional wave forms for the device

Detailed functional description other than parametric performance is published in the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

Other related documents are shown in Table 2.

Table 2. Related Documents

Document Title	Document #
Intel XScale® Processor Developer's Manual	273473
Intel XScale® Microarchitecture Technical Summary	—
Intel® IXP43X Product Line of Network Processors Developer's Manual	316843
Intel® IXP4XX Product Line of Network Processors Specification Update	306428
Intel® IXP400 Software Programmer's Guide	252539
PCI Local Bus Specification, Revision 2.2	N/A
Universal Serial Bus Specification, Revision 1.1	N/A
DDRI Specification	N/A
DDRII Specification	N/A

3.0 Functional Overview

The Intel® IXP43X Product Line of Network Processors is compliant with the Intel® StrongARM* Version 5TE instruction-set architecture (ISA). The IXP43X network processors are designed with Intel 0.13-micron semiconductor process technology. This process technology along with the compactness of the Intel® StrongARM* RISC ISA, which has the ability to simultaneously process data with up to two integrated network processing engines (NPE A and NPE C), and numerous dedicated-function peripheral interfaces enables the IXP43X network processors to operate over a wide range of low cost networking applications with industry-leading performance.

As indicated in Figure 1, Figure 2, Figure 3, Figure 4, and Figure 5, the IXP43X network processors combine many features with the Intel XScale® Processor to create a highly integrated processor applicable to LAN/WAN-based networking applications in addition to other embedded networking applications.

This section describes the main features of the product. For detailed functional description, see the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

Figure 1. Intel® IXP435 Network Processor Block Diagram

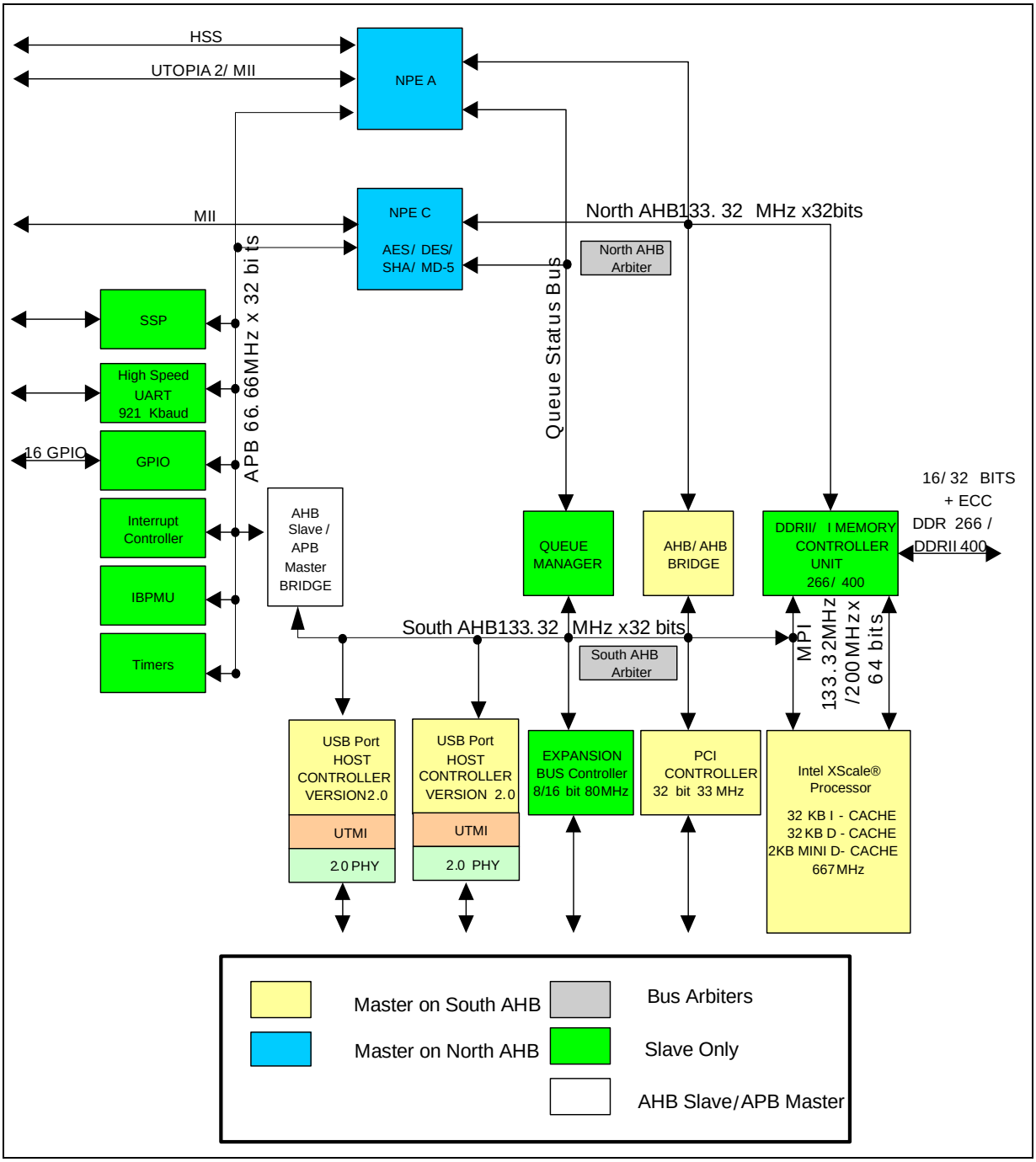


Figure 2. Intel® IXP433 Network Processor Block Diagram

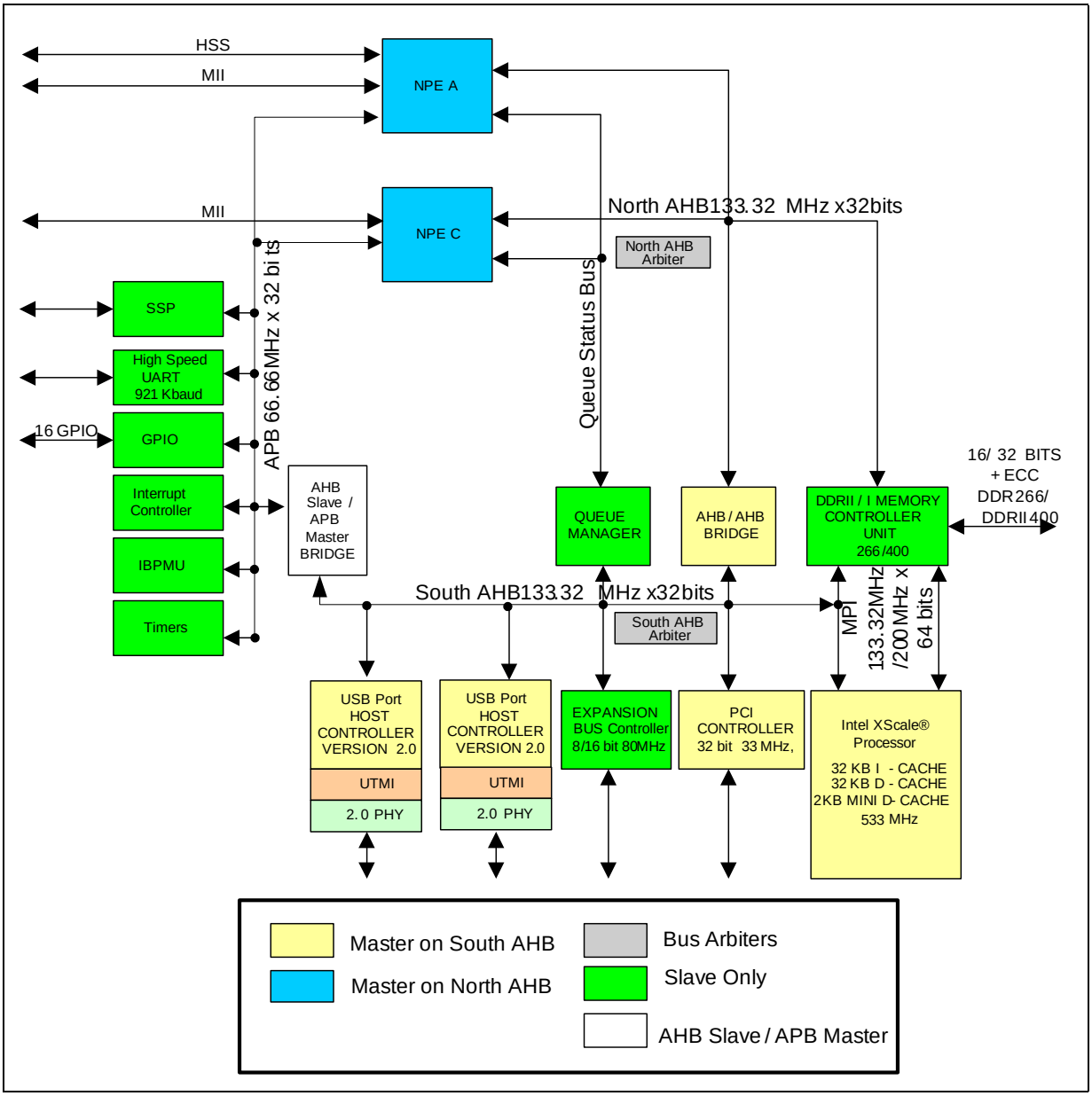


Figure 3. Intel® IXP432 Network Processor Block Diagram

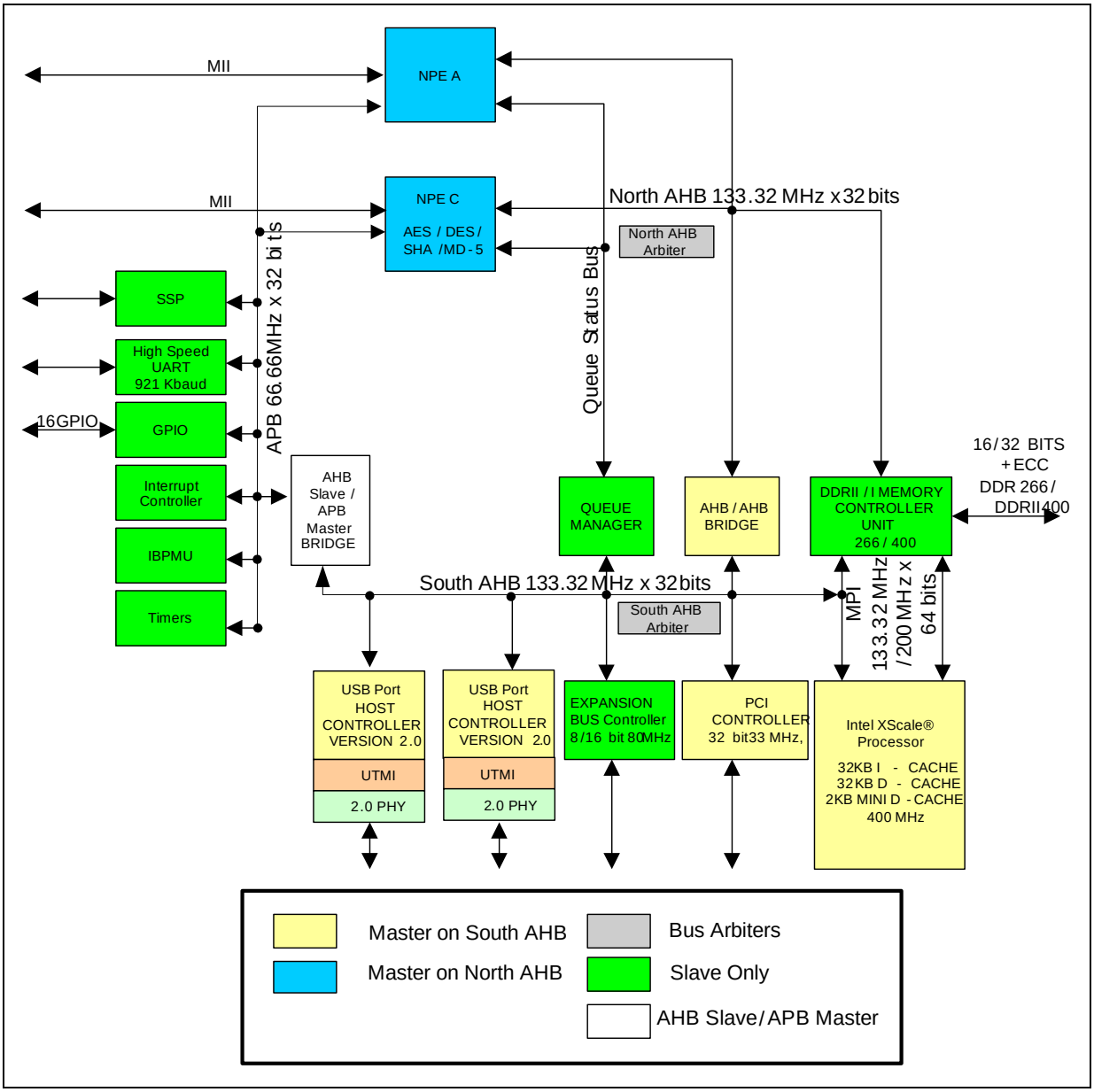


Figure 4. Intel® IXP431 Network Processor Block Diagram

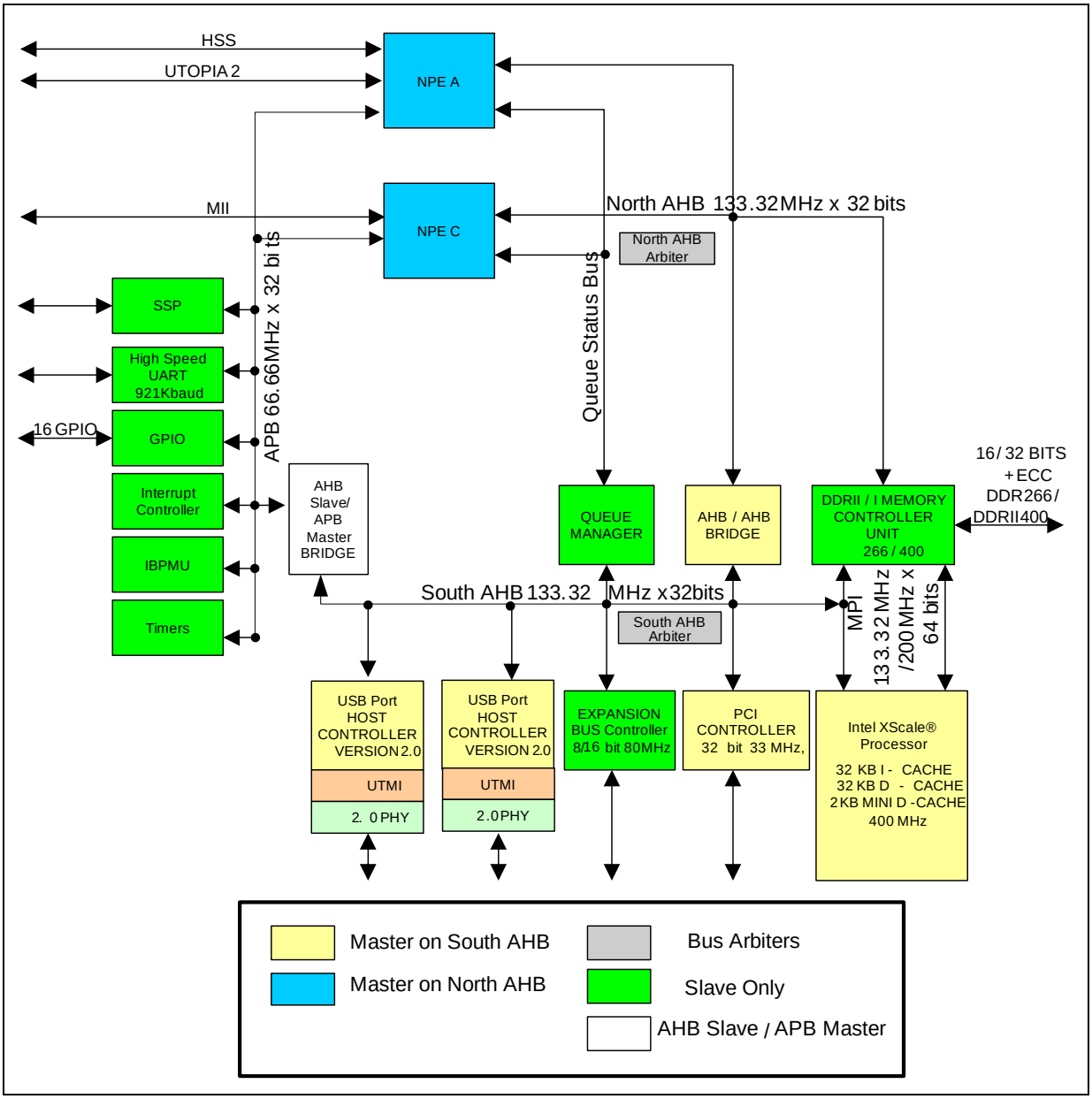
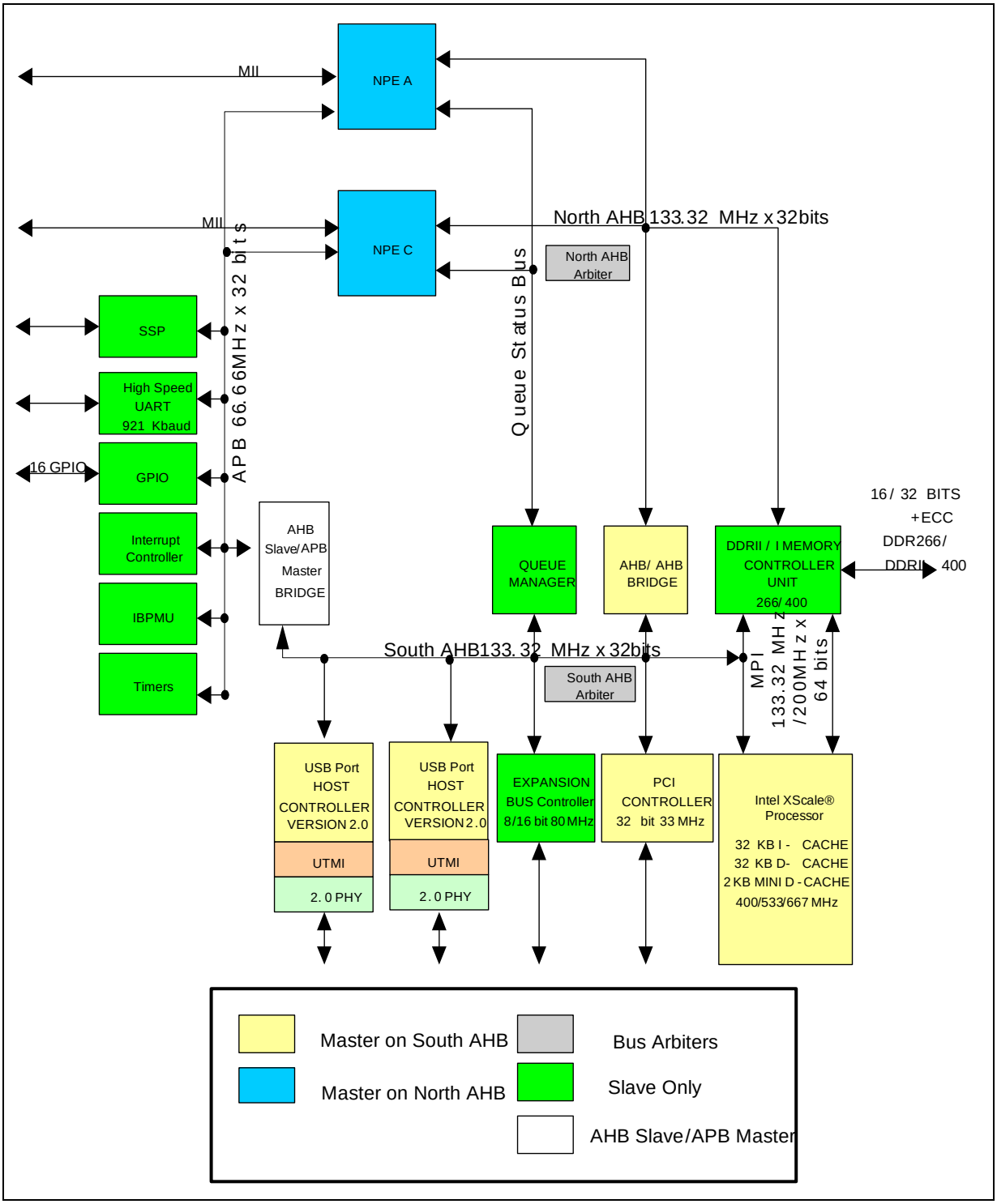


Figure 5. Intel® IXP430 Network Processor Block Diagram



3.1 Key Functional Units

The following sections describe the functional units and their interaction in the system. For more detailed information, refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

Unless otherwise specified, the functional description applies to all the network processors in the IXP43X product line. For specific information on supported interfaces, refer to Table 1 on page 12. For model-specific block diagrams, see Figure 1 on page 14, Figure 2 on page 15, Figure 3 on page 16, Figure 4 on page 17, and Figure 5 on page 18.

3.1.1 Network Processor Engines (NPEs)

The Network Processor Engines (NPEs) are dedicated-function processors containing hardware coprocessors integrated into the IXP43X network processors. The NPEs are used to off-load processing function required by the Intel XScale processor.

These NPEs are high-performance, hardware-multi-threaded processors with additional local hardware assist functionality used to off load highly processor intensive functions such as MII (MAC), CRC checking/generation, AAL segmentation and re-assembly, AES, AES-CCM, DES, 3DES, SHA-1/256/384/512, MD5, and so forth.

All instruction code for the NPEs are stored locally and is accessed using a dedicated instruction memory bus. Similarly, separate dedicated data memory bus allows access to local code store and DDRII/DDRI SDRAM through the AHB bus.

These NPEs support processing of the dedicated peripherals that can include:

- A universal test and operation PHY interface for ATM UTOPIA Level 2 interface
- One high-speed serial (HSS) interface
- Up to two media-independent interface (MII)

Table 3 specifies the possible combination of interfaces for the NPEs contained in the IXP43X network processors. These configurations are determined by the factory programmed fuse settings or by the software that configures the part during boot-up.

Table 3. Network Processor Functions

Device	UTOPIA Level 2	HSS	MII A	MII C	AES / DES / 3DES	HDLC	SHA/ MD-5
Configuration 0	X	X		X	X	4	X
Configuration 1		X	X	X	X	4	X

The NPE core is a hardware-multi-threaded processor engine that is used to accelerate functions that are difficult to achieve high performance in a standard RISC processor. Each NPE core is a 133.32-MHz (or 4*OSC_IN input pin) processor core that has self-contained instruction memory and self-contained data memory that operate in parallel. Each NPE core has 4 K x 29bit of instruction memory and 4 K words of data memory.

In addition to having separate instruction/data memory and local-code store, the NPE core supports hardware multi-threading with support for multiple contexts. The support of hardware multi-threading creates an efficient processor engine with minimal processor stalls due to the ability of the processor core to switch contexts in a single clock cycle, based on a prioritized/preemptive basis. The prioritized/preemptive nature of the context switching allows time-critical applications to be implemented in a low-latency fashion that are required while processing multi-media applications.

The NPE core also connects to several hardware-based coprocessors that are used to implement functions that are difficult for a processor to implement. These functions include:

- HSS serialization/ De-serialization
- DES/3DES/AES
- MD-5
- UTOPIA Level 2 Framing
- CRC checking/generation
- SHA-1/256/384/512
- HDLC bit stuffing/de-stuffing
- Fast Ethernet Media Access Controller functionality

These coprocessors are implemented in hardware, enabling the coprocessors and the NPE processor core to operate in parallel.

The combined forces of the hardware multi-threading, local-code store, independent instruction memory, independent data memory, and parallel processing contained on the NPE allows the Intel XScale processor to be utilized for application purposes. The multi-processing capability of the peripheral interface functions allows unparalleled performance to be achieved by the application running on the Intel XScale processor.

3.1.2 Internal Bus

The internal bus architecture of the IXP43X network processors is designed to allow parallel processing to occur and to isolate bus utilization, based on particular traffic patterns. The bus is segmented into four major buses:

- North advanced, high-performance bus (AHB)
- South AHB
- Memory port interface
- Advanced peripheral bus (APB)

3.1.2.1 North AHB

The North AHB is a 133.32-MHz, 32-bit bus that can be mastered by the NPE A, or NPE C. The targets of the North AHB can be the DDRII/DDRI SDRAM or the AHB/AHB bridge. The AHB/AHB bridge allows the NPEs to access peripherals and internal targets on the South AHB.

Data transfers by the NPEs on the North AHB to the South AHB are targeted predominately to the queue manager. Transfers to the AHB/AHB bridge can be **posted** when writing or **split** when reading.

When a transaction is **posted**, a master on the North AHB requests a write to a peripheral on the South AHB. If the AHB/AHB Bridge has a free FIFO location, the write request is transferred from the master on the North AHB to the AHB/AHB bridge. The AHB/AHB bridge completes a write on the South AHB once it obtains access to the peripheral on the South AHB. The North AHB is released to complete another transaction.

When a transaction is **split**, a master on the North AHB requests a read of a peripheral on the South AHB. If the AHB/AHB bridge has a free FIFO location, the read request is transferred from the master on the North AHB to the AHB/AHB bridge. The AHB/AHB bridge completes a read on the South AHB once it obtains access to the peripheral on the South AHB.

Once the AHB/AHB bridge has obtained the read information from the peripheral on the South AHB, the AHB/AHB bridge notifies the arbiter, on the North AHB, that the AHB/AHB bridge has the data for the master that requested the **split** transfer. The master on the North AHB that requested the **split** transfer arbitrates for the North AHB and

transfers the read data from the AHB/AHB bridge. The North AHB is released to complete another transaction as the North AHB master that requested the split transfer waits for the data to arrive.

These **posting** and **splitting** transfers allow control of the North AHB to be given to another master on the North AHB enabling the North AHB to achieve maximum efficiency. Transfers to the AHB/AHB bridge are considered to be small and infrequent, relative to the traffic passed between the NPEs and the DDRII/DDRI SDRAM on the North AHB.

When multiple masters arbitrate for the North AHB, the masters are awarded access to the bus in a round-robin fashion. Each transaction is no longer than an eight-word burst. This implementation promotes fairness within the system.

3.1.2.2 South AHB

The South AHB is a 133.32-MHz (that is 4*OSC_IN input pin), 32-bit bus that can be mastered by the Intel XScale processor, PCI controller, USB Host Controller, and the AHB/AHB bridge. The targets of the South AHB Bus can be the DDRII/DDRI SDRAM, PCI Controller, Queue Manager, Expansion Bus, or the AHB/APB bridge.

Accessing across the APB/AHB bridge allows interfacing to peripherals attached to the APB. The Expansion bus and PCI controller can be configured to support split transfers.

Arbitration on the South AHB are round-robin. Each transaction to be no longer than an eight-word burst. This implementation promotes fairness within the system.

3.1.2.3 Memory Port Interface

The Memory Port Interface (MPI) is a 64-bit bus that provides the Intel XScale processor a dedicated interface to the DDRII/DDRI SDRAM. The Memory Port Interface operates at 133.32 MHz when DDRI SDRAM is used, and 200 MHz when DDRII SDRAM is used

The Memory Port Interface stores memory transactions from the Intel XScale processor, which have not been processed by the Memory Controller. The Memory Port Interface supports eight core processor read transactions up to 32 bytes each. That total equals the maximum number of outstanding transaction the Core Processor Bus Controller can support. (That includes core DCU [4 - load requests to unique cache lines], IFU [2 - prefetch], IMM [1 - tablewalk], DMM [1 - tablewalk].)

The Memory Port Interface also supports eight core-processor-posted write transactions up to 16 bytes each.

Arbitration on the Memory Port Interface is not required due to no contention with other masters. Arbitration exists in the DDRII/DDRI memory controller between all of the main internal busses.

3.1.2.4 APB Bus

The APB Bus is a 66.66-MHz, 32-bit bus that is mastered by the AHB/APB bridge only. The targets of the APB bus are:

- Timers
- UART

- The internal bus performance monitoring unit (IBPMU)
- GPIOs
- Synchronous Peripheral Port Interface
- All NPEs
- Interrupt controller

The APB interface is also used as an alternate-path interface to the NPEs and is used for NPE code download and configuration.

No arbitration is required due to a single master implementation.

3.1.3 MII Interfaces

The IXP43X product line of network processors can be configured to support up to two industry-standard MII interfaces. These interfaces are integrated into the IXP43X network processors with separate media-access controllers and in many cases independent network processing engines. Refer Table 3 for allowable combinations.

The independent NPEs and MACs allow parallel processing of data traffic on the MII interfaces and off loading of processing required by the Intel XScale processor. The IXP43X network processors are compliant with IEEE 802.3 specification.

In addition to the MII interfaces, the IXP43X network processors includes a single management data interface that is used to configure and control PHY devices that are connected to the MII interfaces.

3.1.4 UTOPIA Level 2 Interface

The integrated UTOPIA Level 2 interface works with a network-processing engine core for several of the IXP43X network processors. The pins of the UTOPIA Level 2 interface are multiplexed with one of the MII interfaces. Refer Table 3 for additional information.

The UTOPIA Level 2 interface supports a single- or a multiple-physical-interface configuration with cell-level or octet-level handshaking. The network processing engine handles segmentation and reassembly of ATM cells, CRC checking/generation, and transfer of data to/from memory. This allows parallel processing of data traffic on the UTOPIA Level 2 interface, off-loading these processing tasks from the Intel XScale processor.

The IXP43X network processors are compliant with the ATM Forum, *UTOPIA Level-2 Specification*, Revision 1.0.

3.1.5 USB Version 2.0 Host Interface

USB Host functionality is implemented on the IXP43X network processors. The function being performed is defined by the USB 2.0 specification, maintained by usb.org and the interface is EHCI compliant, as defined by Intel.

Supported features are:

- Host function
- Low-speed interface
- Full-speed interface
- High-speed interface
- EHCI register interface
- UTMI+ Level 2 Compliant

The following is a partial list of features that are not supported:

- Device function
- OTG function

3.1.6 PCI Controller

The PCI controller in the IXP43X network processors is compatible with the *PCI Local Bus Specification*, Rev. 2.2. The PCI interface is 32-bit compatible bus and capable of operating as either a host or an option (that is, not the Host). This PCI implementation supports 3.3 V I/O and 33 MHz only.

3.1.7 DDRII/DDRI Memory Controller

The IXP43X network processors integrate a high-performance, multi-ported Memory Controller Unit (MCU) to provide a direct interface between IXP43X network processors and their local memory subsystem. The MCU supports:

- DDRI 266 or DDRII-400 SDRAM
- 128/256/512-Mbit, 1-Gbit DDRI SDRAM technology support
- Supports 256/512-Mbit technologies for DDRII-400
- Only unbuffered DRAM support (No registered DRAM support)
- Dedicated port for Intel XScale processor to DDRII/DDRI SDRAM
- Between 32 MBs and 1-GB of 32-bit DDRI SDRAM
- Between 64MBs and 512 MBs of 32-bit DDRII SDRAM
- 16MB for 16-bit memory systems for DDRI SDRAM (non-ECC) supporting 128-Mbit technology only
- 32MB for 16-bit memory systems for DDRII SDRAM (non-ECC) supporting 256-Mbit technology only
- Single-bit error correction, multi-bit detection support (ECC)
- 32-bit, 40-bit wide memory interfaces (non-ECC and ECC support), and 16-bit wide memory interfaces (non-ECC)

The DDRII/DDRI SDRAM interface provides a direct connection to a high-bandwidth and reliable memory subsystem. The DDRII/DDRI SDRAM interface is a 16 or 32-bit-wide data path.

An 8-bit Error Correction Code (ECC) across each 32-bit word improves system reliability. It is important to note that ECC is also referred to as CB in many DIMM specifications. The pins on the IXP43X network processors are called DDR_CB[7:0]. ECC is only implemented in the 32-bit mode of operation. The algorithm used to generate the 8-bit ECC is implemented over 64-bit.

The ECC circuitry is designed to operate always on a 64-bit data and when operating in 32-bit mode, the upper 32 bits are driven to zeros internally. To summarize the impact to the customer, the full 8 bits of ECC is stored and read from a memory array for the ECC logic to work. An 8-bit-wide memory is used when implementing ECC.

The memory controller only corrects single bit ECC errors on read cycles. The ECC is stored into the DDRII/DDRI SDRAM array along with the data and is checked when the data is read. If the code is incorrect, the MCU corrects the data (if possible) before reaching the initiator of the read. ECC error scrubbing is done with software. User-defined fault correction software is responsible for scrubbing the memory array and handling double-bit errors.

To limit double-bit errors from occurring, periodically reading the entire usable memory array allows the hardware unit within the memory controller to correct any single-bit, ECC errors that may have occurred prior to these errors becoming double-bit ECC errors. Implementing this method is system-dependent.

It is important to note that when sub-word writes (byte writes or half-word writes within a
word-aligned boundary) are done to a 32-bit memory with ECC enabled, the memory controller performs read-modify writes. There is a performance impact with read-modify writes that must be considered when writing software.

With read-modify writes, the memory controller reads the 32-bit word that encompasses the byte that is to be written when a byte write is requested. The memory controller modifies the specified byte, calculates a new ECC, and writes the entire 32-bit word back into the memory location it was read from.

The value written back into the memory location contains the 32-bit word with the modified byte and the new ECC value.

The MCU supports two physical banks of DDRII/DDRI SDRAM. The MCU has support for unbuffered DDRI 266 and DDRII 400 in the form of discrete chips only.

The MCU supports a memory subsystem ranging from 32 MB to 1 GB for 32-bit memory systems for DDRI SDRAM, from 64 MB to 512 MB for 32-bit memory systems for DDRII SDRAM, and supports 16 MB for 16-bit memory systems for DDRI SDRAM (non-ECC), and 32 MB for 16-bit memory systems for DDRII SDRAM (non-ECC). An ECC or non-ECC system can be implemented using x8, or x16 devices. Table 4, Table 5, Table 6 and Table 7 illustrate the supported DDRII/DDRI SDRAM configurations

The two DDRII/DDRI SDRAM chip enables (DDR_CS_N[1:0]) support a DDRII/DDRI SDRAM memory subsystem consisting of two banks. The base address for the two contiguous banks are programmed in the DDRII/DDRI SDRAM Base Register (SDBR) and is aligned to a 16 MB boundary. The size of each DDRII/DDRI SDRAM bank is programmed with the DDRII/DDRI SDRAM boundary registers (SBR0 and SBR1).

The DDRII/DDRI SDRAM devices comprise four internal leaves. The MCU controls the leaf selects within DDRII/DDRI SDRAM by toggling DDR_BA[0] and DDR_BA[1].

Table 4. Supported DDRI 32-bit SDRAM Configurations (Sheet 1 of 2)

DDR SDRAM Technology	DDR SDRAM Arrangement	# Banks	Address Size		Leaf Select		Total Memory Size[a]	Page Size[b]
			Row	Column	DDR_BA[1]	DDR_BA[0]		
128 Mbit[c]	16 M x 8	1	12	10	ADDR[26]	ADDR[25]	64 M	4KB
		2					128 M	4KB
	8 M x 16	1	12	9	ADDR[25]	ADDR[24]	32 M	2KB
		2					64 M	2KB
256 Mbit	32 M x 8	1	13	10	ADDR[27]	ADDR[26]	128 M	4KB
		2					256 M	4KB
	16 M x 16	1	13	9	ADDR[26]	ADDR[25]	64 M	2KB
		2					128 M	2KB
512 Mbit	64 M x 8	1	13	11	ADDR[28]	ADDR[27]	256 M	8KB
		2					512 M	8KB
	32 M x 16	1	13	10	ADDR[27]	ADDR[26]	128 M	4KB
		2					256 M	4KB

Table 4. Supported DDRI 32-bit SDRAM Configurations (Sheet 2 of 2)

DDR SDRAM Technology	DDR SDRAM Arrangement	# Banks	Address Size		Leaf Select		Total Memory Size[a]	Page Size[b]
			Row	Column	DDR_BA[1]	DDR_BA[0]		
1 Gbit[c]	128 M x 8	1	14	11	**ADDR[29]**	**ADDR[28]**	512 M	8KB
		2					1 G	8KB
	64 M x 16	1	14	10	**ADDR[28]**	**ADDR[27]**	256 M	4KB
		2					512 M	4KB

a. Table indicates 32-bit wide memory subsystem sizes.
b. Table indicates 32-bit wide memory page sizes.
c. Supported with DDR SDRAM only

Table 5. Supported DDRII 32-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	32M x 8	1	13	10	ADDR[27]	ADDR[26]	128MB	4KB
		2					256MB	4KB
	16M x16	1	13	9	ADDR[26]	ADDR[25]	64MB	2KB
		2					128MB	2KB
512 Mbit	64M x 8	1	14	10	ADDR[28]	ADDR[27]	256MB	4KB
		2					512MB	4KB
	32M x16	1	13	10	ADDR[27]	ADDR[26]	128MB	4KB
		2					256MB	4KB

Table 6. Supported DDRI 16-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
128 Mbit	8M x16	1	12	9	ADDR[23]	ADDR[22]	16MB	1KB

Table 7. Supported DDRII 16-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# of Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	16M x16	1	13	9	ADDR[24]	ADDR[23]	32MB	1KB

The memory controller internally interfaces with the North AHB, South AHB, and Memory Port Interface with independent interfaces. This architecture allows DDRII/DDRI SDRAM transfers to be interleaved and pipelined to achieve maximum possible efficiency.

The MCU supports DDRII/DDRI SDRAM burst length of four for 32-bit and 16-bit data bus width options. A burst length of four enables seamless read/write bursting of long data streams as long as the memory transaction does not cross the page boundary. Page boundaries are at naturally aligned boundaries. The MCU ensures that the page boundary is not crossed within a single transaction by initiating a disconnect at next ADB (128-byte address boundary) on the internal bus prior to the page boundary.

The programming priority of the MCU is for the Memory Port Interface to have the highest priority and two AHB ports has the next highest priority. For more information on MCU arbitration support and configuration see the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

One item to be aware of is that when ECC is being used, the memory chip chosen to support the ECC must match that of the technology chosen on the interface. Therefore, if x8 in a given configuration technology is chosen then the ECC memory chip is the same. If a x16 configuration is chosen then a x16 chip is to be used for the ECC chip.

3.1.8 Expansion Interface

The expansion interface allows easy and in most cases glue-less connection to peripheral devices. It also provides input information for device configuration after reset.

Some of the peripheral device types are Intel multiplexed, Intel non-multiplexed, Intel StrataFlash®, Synchronous Intel StrataFlash® Memory, Motorola* multiplexed and Motorola* non-multiplexed target devices.

The expansion interface functions support 8-bit or 16-bit data operation and allows an address range of 512 bytes to 16 MBs, using 24 address lines for each of the four independent chip selects.

Access to the expansion-bus interface is completed in five phases. Each of the five phases can be lengthened or shortened by setting various configuration registers on a per-chip-select basis. This feature allows the IXP43X network processors to connect to a wide variety of peripheral devices with varying speeds.

The expansion interface supports Intel or Motorola* microprocessor-style bus cycles. The bus cycles can be configured to be multiplexed address/data cycles or separate address/data cycles for each of the four chip-selects.

The expansion interface is an asynchronous interface to externally connected chips. A clock is supplied to the IXP43X network processors expansion interface for proper operation. This clock can be driven from GPIO 15 or an external source. Devices on the expansion bus can be clocked by an external clock at a rate of up to 80 MHz. If GPIO 15 is used as the clock source, the Expansion Bus interface can only be clocked at a maximum of 33.33 MHz. GPIO 15's maximum clock rate is 33.33 MHz.

3.1.9 High-Speed Serial Interface

The high-speed serial interface (HSS) is a six-signal interface that support serial transfer speeds from 512 KHz to 8.192 MHz, for some of the IXP43X network processors.

The interface allows direct connection of up to four T1/E1 framers and CODEC/SLICs to the IXP43X network processors. The high-speed, serial interface is capable of supporting various protocols, based on the implementation of the code developed for the network processor engine core.

For a list of supported protocols, see the *Intel® IXP400 Software Programmer's Guide*.

3.1.10 UART Interface

The UART interface is a 16550-compliant UART with the exception of transmit and receive buffers. Transmit and receive buffers are 64 bytes-deep versus the 16 bytes required by the 16550 UART specification.

The interface can be configured to support speeds from 1,200 Baud to 921 Kbaud. The interface supports the following configurations:

- Five, six, seven, or eight data-bit transfers
- One or two stop bits
- Even, odd, or no parity

The request-to-send (RTS0_N) and clear-to-send (CTS0_N) modem control signals also are available with the interface for hardware flow control.

3.1.11 GPIO

16 GPIO pins are supported by the IXP43X network processors. The GPIO pins 0 through 15 can be configured to be general-purpose input or general-purpose output. Additionally, GPIO pins 0 through 12 can be configured to be an interrupt input.

GPIO Pin 1 can also be configured as a clock input for an external USB 2.0 Host Bypass clock. When spread spectrum clocking (SSC) is used, an external clock should be used as the source for the USB 2.0 Host clock. Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for more information.

GPIO Pin 14 and GPIO 15 can also be configured as a clock output. The output-clock configuration can be set at various speeds, up to 33.33 MHz, with various duty cycles. GPIO Pin 14 is configured as an input, upon reset. GPIO Pin 15 is configured as an output, upon reset. GPIO Pin 15 can be used to clock the expansion interface, after reset.

Table 8. GPIO Alternate Function Table

GPIO Pin Number	GPIO function	Alternate Function
0	General purpose input/output or interrupt source	Reserved
1†	General purpose input/output or interrupt source	External USB 48 MHz Bypass Clock
2	General purpose input/output or interrupt source	Reserved
3	General purpose input/output or interrupt source	Reserved
4	General purpose input/output or interrupt source	Reserved
5	General purpose input/output or interrupt source	Reserved
6	General purpose input/output or interrupt source	Reserved
7	General purpose input/output or interrupt source	Reserved
8	General purpose input/output or interrupt source	Reserved
9:12	General purpose input/output or interrupt source	Reserved
13	General purpose input/output	Reserved
14	General purpose input/output or output clock	Output clock 14
15	Output Clock or General purpose input/output	Output clock 15
†	When a spread spectrum clock is used, GPIO Pin 1 should be configured as an input clock for USB Host. See the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for detailed information.	

3.1.12 Internal Bus Performance Monitoring Unit (IBPMU)

The IXP43X network processors contain a performance monitoring unit that can be used to capture predefined events within the system outside of the Intel XScale processor. These features aid in measuring and monitoring various system parameters that contribute to the overall performance of the processor.

The Performance Monitoring (PMON) facility provided comprises:

- Eight Programmable Event Counters (PECx) clocked by AHB clock(133MHz)
- Eight Programmable Event Counters (MPECx) clocked by MCU clock(133MHz/ 200MHz)
- Previous Master/Slave Register
- Event Selection Multiplexor
- Simultaneous event counting

The programmable event counters are 27 bits wide. Each counter can be programmed to observe one event from a defined set of events. An event consists of a set of parameters that define a start condition and a stop condition.

The monitored events are selected by programming the Event Select Registers (ESR).

3.1.13 Interrupt Controller

The IXP43X network processors implement up to 64 interrupt sources to allow an extension of the FIQ and IRQ interrupt sources of Intel XScale processor. These sources can originate from some external GPIO pins, internal peripheral interfaces, or internal logic.

The interrupt controller can configure each interrupt source as an FIQ, IRQ, or disabled. The interrupt source are prioritize in an ascending order.For example, Interrupt 0 has higher priority than 1,Interrupt 8 has a higher priority than 9, 9 has a higher priority than 10, and 30 has a higher priority that 31.

Additionally, the interrupt sources tied to Interrupt 0 to 7 can be prioritized. For example, Interrupt 7 can be prioritize over Interrupt 0.

3.1.14 Timers

The IXP43X network processors contain four internal timers operating at 66.66 MHz (that is 2*OSC_IN input pin) that allows task scheduling and prevent software lock-ups. The device has four 32-bit counters:

- Watch-Dog Timer
- Timestamp Timer
- Two general-purpose Timers

The Timestamp Timer and the two general-purpose timers have the optional ability to use a pre-scaled clock. A programmable pre-scaler can be used to divide the input clock by a 16-bit value. The input clock can be either the APB clock (66.66 MHz) or a 20-ns version of the APB clock (50 MHz). By default all timers use the APB clock.

The 16-bit pre-scale value ranges from divide by 2 to 65,536 and results in a new clock enable available for the timers that ranges from 33.33 MHz down to 1,017.26 Hz.

The Timestamp Timer also contains a 32-bit compare register that allows an interrupt to be created at times other than time 0.

3.1.15 Synchronous Serial Port Interface

The IXP43X network processors have a dedicated Synchronous Serial Port (SSP) interface. The SSP interface is a full-duplex synchronous serial interface. It can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom CODECs, and many other devices that use serial protocols for transferring data.

It supports National's Microwire, Synchronous Serial Protocol (SSP) of Texas Instruments*, and Serial Peripheral Interface (SPI) protocol of Motorola*.

The SSP operates in master mode (the attached peripheral functions as a slave), and supports serial bit rates from 7.2 Kbps to 1.8432 Mbps using the on-chip, 3.6864-MHz clock. Serial data formats may range from 4 to 16 bits in length. Two on-chip register blocks function as independent FIFOs for data, one for each direction. The FIFOs are 16 entries deep x 16 bits wide. Each 32-bit word from the system fills one entry in a FIFO using the lower half 16-bits of a 32-bit word.

3.1.16 AES/DES/SHA/MD-5

The IXP43X network processors implement chip hardware acceleration for underlying security and authentication algorithms.

The encryption/decryption algorithms supported are AES, single pass AES-CCM, DES, and triple DES. These algorithms are commonly found when implementing IPSEC, VPN, WEP, WEP2, WPA, and WPA2.

The authentication algorithms supported are MD-5, SHA-1, SHA-256, SHA-384, and SHA-512. Inclusion of SHA-384 and SHA-512 allows 256-bit key authentication to pair up with 256-bit AES support.

3.1.17 Queue Manager

The Queue Manager provides a means for maintaining coherency for data handling between various processor cores contained on the IXP43X network processors (NPE to NPE, NPE to Intel XScale processor, and so on). It maintains the queues as circular buffers in an embedded 8-Kbyte SRAM. The Queue Manager also implements the status flags and pointers required for each queue.

The Queue Manager manages 64 independent queues. Each queue can be configured for buffer and entry size. Additionally status flags are maintained for each queue.

The Queue Manager interfaces include an Advanced High-performance Bus (AHB) interface to the NPEs and Intel XScale processor (or any other AHB bus master), a Flag Bus interface, an event bus (to the NPE condition select logic), and two interrupts to the Intel XScale processor.

The AHB interface is used for configuration of the Queue Manager and provides access to queues, queue status, and SRAM. Individual queue status for queues 0-31 is communicated to the NPEs through the flag bus. Combined queue status for queues 32-63 are communicated to the NPEs through the event bus. The two interrupts, one for queues 0-31 and one for queues 32-63, provide status interrupts to the Intel XScale processor.

3.2 Intel XScale® Processor

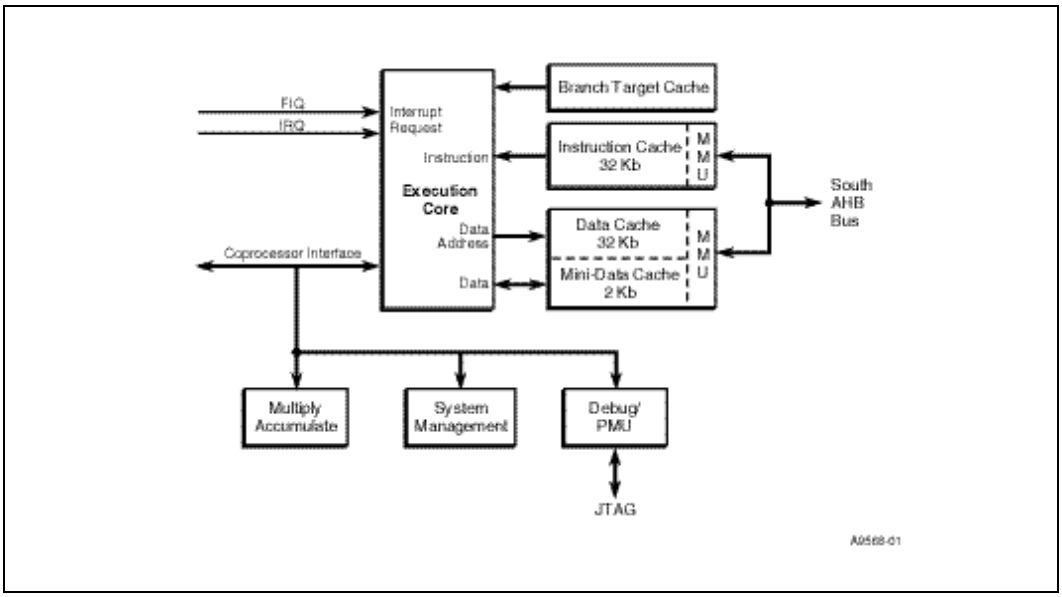
The Intel XScale technology is compliant with the Intel® StrongARM* Version 5TE instruction-set architecture (ISA). The Intel XScale processor, shown in Figure 6, is designed with Intel 0.13-micron production semiconductor process technology. This process technology, with the compactness of the Intel® StrongARM* RISC ISA enables the Intel XScale processor to operate over a wide speed and power range, producing industry-leading mW/MIPS performance.

The features of the Intel XScale processor include:

- Seven/eight-stage super-pipeline promotes high-speed, efficient core performance

- 128-entry branch target buffer keeps pipeline filled with statistically correct branch choices
- 32-entry instruction memory-management unit for logical-to-physical address translation, access permissions, and Instruction-Cache (I-cache) attributes
- 32-entry data-memory management unit for logical-to-physical address translation, access permissions, Data-Cache (D-Cache) attributes
- 32-Kbyte instruction cache can hold entire programs, preventing core stalls caused by multi-cycle memory access
- 32-Kbyte data cache reduces core stalls caused by multi-cycle memory accesses
- 2-Kbyte mini-data cache for frequently changing data streams avoids **thrashing** of the D-cache
- Four-entry, fill-and-pend buffers to promote core efficiency by allowing **hit-under-miss** operation with data caches
- Eight-entry write buffer allows the core to continue execution while writing data to memory
- Multiple-accumulate coprocessor that can do two simultaneous, 16-bit, SIMD multiplies with 40-bit accumulation for efficient, high-quality media and signal processing
- Performance monitoring unit (PMU) furnishing four 32-bit event counters and one 32-bit cycle counter for analysis of hit rates, and so on.
  This PMU is for the Intel XScale processor only. An additional PMU is supplied for monitoring of internal bus performance.
- JTAG debug unit that uses hardware break points and 256-entry trace history buffer (for flow-change messages) to debug programs

Figure 6. Intel XScale® Technology Block Diagram



3.2.1 Super Pipeline

The super pipeline comprises integer, multiply-accumulate (MAC), and memory pipes.

The integer pipe has seven stages:

- Branch Target Buffer (BTB)/Fetch 1
- Fetch 2
- Decode
- Register File/Shift
- ALU Execute
- State Execute
- Integer Writeback

The memory pipe has eight stages:

- The first five stages of the Integer pipe explained above (that is, BTB/Fetch 1 to ALU Execute) and ends with the following three memory stages:
  - Data Cache 1
  - Data Cache 2
  - Data Cache Writeback
  - The MAC pipe has six to nine stages:
- The first four stages of the Integer pipe explained above (that is, BTB/Fetch 1 to ALU Execute) and ends with the following MAC stages:
  - MAC 1
  - MAC 2
  - MAC 3
  - MAC 4
  - Data Cache Writeback

The MAC pipe supports a data-dependent early terminate where stages MAC 2, MAC 3, and/or MAC 4 are bypassed.

Deep pipes promote high instruction execution rates only when there is a way to predict successfully the outcome of branch instructions. The branch target buffer provides this way.

3.2.2 Branch Target Buffer

Each entry of the 128-entry Branch Target Buffer (BTB) contains address of a branch instruction, the target address associated with the branch instruction, and previous history of the branch being taken or not taken. The history is recorded as one of the following four states:

- Strongly taken
- Weakly taken
- Weakly not taken
- Strongly not taken

The BTB can be enabled or disabled through Coprocessor 15, Register 1.

When the address of the branch instruction hits in the BTB and its history is strongly or weakly taken, the instruction at the branch target address is fetched. When its history is not taken strongly or weakly, the next sequential instruction is fetched. In either case the history is updated.

Data associated with a branch instruction enters the BTB the first time the branch is taken. This data enters the BTB in a slot with a history of strongly not-taken. That is it overwrites the existing data.

Successfully predicted branches avoid any branch-latency penalties in the super pipeline. Unsuccessfully predicted branches result in a four-to-five-cycle branch-latency penalty in the super pipeline.

3.2.3 Instruction Memory Management Unit

For instruction pre-fetches, the Instruction Memory Management Unit (IMMU) controls logical-to-physical address translation, memory access permissions, memory-domain identifications, and attributes. Governing operation of the instruction cache are categorized as attributes.

The IMMU contains a 32-entry, fully associative instruction-translation, look-aside buffer (ITLB) that has a round-robin replacement policy. ITLB entries zero through 30 can be locked.

When an instruction pre-fetch **misses** in the ITLB, the IMMU invokes an automatic table-walk mechanism that fetches an associated descriptor from memory and loads it into the ITLB. The descriptor contains information for logical-to-physical address translation, memory-access permissions, memory-domain identifications, and attributes governing operation of the I-cache. The IMMU then continues the instruction pre-fetch by using the address translation just entered into the ITLB. When an instruction pre-fetch hits in the ITLB, the IMMU continues the pre-fetch using the address translation already resident in the ITLB.

Access permissions for each up to 16 memory domains can be programmed. When an instruction pre-fetch is attempted to an area of memory in violation of access permissions, the attempt is aborted and a pre-fetch abort is sent to the core for exception processing. You can either enable or disable the IMMU and DMMU together.

3.2.4 Data Memory Management Unit

For data fetches, the Data Memory Management Unit (DMMU) controls logical-to-physical address translation, memory-access permissions, memory-domain identifications, and attributes. Governing operation of the data cache or mini-data cache and write buffer are categorized as attributes. The DMMU contains 32-entry, fully associative data-translation, look-aside buffer (DTLB) that has a round-robin replacement policy. DTLB entries 0 through 30 can be locked.

When a data fetch **misses** in the DTLB, the DMMU invokes an automatic table-walk mechanism that fetches an associated descriptor from memory and loads it into the DTLB. The descriptor contains information for logical-to-physical address translation, memory-access permissions, memory-domain identifications, and attributes (governing operation of the D-cache or mini-data cache and write buffer).

The DMMU continues the data fetch by using the address translation just entered into the DTLB. When a data fetch hits in the DTLB, the DMMU continues the fetch using the address translation already resident in the DTLB.

Access permissions for each of up to 16 memory domains can be programmed. When a data fetch is attempted to an area of memory in violation of access permissions, the attempt is aborted and a data abort is sent to the core for exception processing.

You can either enable or disable the IMMU and DMMU together.

3.2.5 Instruction Cache

The Instruction Cache (I-Cache) can contain high-use, multiple-code segments or entire programs, allowing core access to instructions at core frequencies. This prevents core stalls, caused by
multi-cycle accesses to external memory.

The 32-Kbyte I-cache is 32-set/32-way associative, where each set contains 32 ways and each way contains a tag address, a cache line of instructions (eight 32-bit words and one parity bit per word), and a line-valid bit. For each of the 32 sets, 0 through 28 ways can be locked. Unlocked ways are replaceable through round-robin policy.

The I-cache can be enabled or disabled. Attribute bits within the descriptors contained in the ITLB of the IMMU provide some control over an enabled I-cache.

When a needed line (eight 32-bit words) is not present in the I-cache, the line is fetched (critical word first) from memory through a two-level, deep-fetch queue. The fetch queue allows the next instruction to be accessed from the I-cache only when its data operands do not depend on the execution results of the instruction being fetched through the queue.

3.2.6 Data Cache

The 32-Kbyte D-cache is 32-set/32-way associative, where each set contains 32 ways and each way contains a tag address, a cache line (32 bytes with one parity bit per byte) of data, two dirty bits (one for each of two eight-byte groupings in a line), and one valid bit. For each of the 32 sets, zero through 28 ways can be locked, unlocked, or used as local SRAM. Unlocked ways are replaceable through a round-robin policy.

The D-cache (together with the mini-data cache) can be enabled or disabled. Attribute bits within the descriptors, contained in the DTLB of the DMMU, provide significant control over an enabled D-cache. These bits specify cache operating modes such as read and write allocate, write-back, write-through, and D-cache versus mini-data cache targeting.

The D-cache (and mini-data cache) work with the load buffer and pend buffer to provide **hit-under-miss** capability that allows the core to access other data in the **cache after a miss** is encountered. The D-cache (and mini-data cache) works in conjunction with the write buffer for data that is to be stored to memory.

3.2.7 Mini-Data Cache

The mini-data cache can contain frequently changing data streams such as MPEG video, allowing the core access to data streams at core frequencies. This prevents core stalls, caused by multi-cycle access to external memory. The mini-data cache relieves the D-cache of data **thrashing** caused by frequently changing data streams.

The 2-Kbyte, mini-data cache is 32-set/two-way associative, where each set contains two ways and each way contains a tag address, a cache line (32 bytes with one parity bit per byte) of data, two dirty bits (one for each of two eight-byte groupings in a line), and a valid bit. The mini-data cache uses a round-robin replacement policy, and cannot be locked.

The mini-data cache (together with the D-cache) can be enabled or disabled. Attribute bits contained within a coprocessor register specify operating modes write and/or read allocate, write-back, and write-through.

The mini-data cache (and D-cache) work with the load buffer and pend buffer to provide **hit-under-miss** capability that allows the core to access other data in the cache after a **miss** is encountered. The mini-data cache (and D-cache) works in conjunction with the write buffer for data that is to be stored to memory.

3.2.8 Fill Buffer and Pend Buffer

The four-entry fill buffer (FB) works with the core to hold non-cacheable loads till the bus controller acts on them. The FB and the four-entry pend buffer (PB) work with the D-cache and mini-data cache to provide **hit-under-miss** capability, allowing the core to seek other data in the caches as **miss** data is being fetched from memory.

The FB can contain up to four unique **miss** addresses (logical), allowing four **misses** before the core is stalled. The PB holds up to four addresses (logical) for additional **misses** to those addresses that are already in the FB. A coprocessor register can specify draining of the fill and pend (write) buffers.

3.2.9 Write Buffer

The write buffer (WB) holds data for storage to memory until the bus controller can act on it. The WB is eight entries deep, where each entry holds 16 bytes. The WB is constantly enabled and accepts data from the core, D-cache, or mini-data cache.

Coprocessor 15, Register 1 specifies whether WB coalescing is enabled or disabled. When coalescing is disabled, storage to memory occur in program order, regardless of the attribute bits within the descriptors located in the DTLB.

When coalescing is enabled, the attribute bits within the descriptors located in the DTLB are examined to determine whether coalescing is enabled for the destination region of memory. When coalescing is enabled in both CP15, R1 and the DTLB, data that enters the WB can coalesce with any of the eight entries (16 bytes) and stored to the destination memory region, but not in the program order.

Stores to a memory region specified to be non-cacheable and non-bufferable by the attribute bits within the descriptors located in the DTLB causes the core to stall until the store completes. A coprocessor register can specify draining of the write buffer.

3.2.10 Multiply-Accumulate Coprocessor

For efficient processing of high-quality, media-and-signal-processing algorithms, the Multiply-Accumulate Coprocessor (CP0) provides 40-bit accumulation of 16 x 16, dual-16 x 16 (SIMD), and 32 x 32 signed multiplies. Special MAR and MRA instructions are implemented to move the 40-bit accumulator to two core-general registers (MAR) and move two core-general registers to the 40-bit accumulator (MRA). The 40-bit accumulator can be stored or loaded to or from D-cache, mini-data cache, or memory using two STC or LDC instructions.

The 16 x 16 signed multiply-accumulates (MIAxy) multiply either the high/high, low/low, high/low, or low/high 16 bits of a 32-bit core general register (multiplier) and another 32-bit core general register (multiplicand) to produce a full, 32-bit product that is sign-extended to 40 bits and added to the 40-bit accumulator.

Dual-signed, 16 x 16 (SIMD) multiply-accumulates (MIAPH) multiply the high/high and low/low 16-bits of a packed 32-bit, core-general register (multiplier) and another packed 32-bit, core-general register (multiplicand) to produce two 16-bits products that are both sign-extended to 40 bits and added to the 40-bit accumulator.

The 32 x 32 signed multiply-accumulates (MIA) multiply a 32-bit, core-general register (multiplier) and another 32-bit, core-general register (multiplicand) to produce a 64-bit product where the 40 LSBs are added to the 40-bit accumulator. The 16 x 32 versions of the 32 x 32 multiply-accumulate instructions complete in a single cycle.

3.2.11 Performance Monitoring Unit

The Performance Monitoring Unit (PMU) comprises four 32-bit performance counters that allows four unique events to be monitored simultaneously and one 32-bit clock counter that can be used in conjunction with the performance counters. The main purpose of the clock counter is to count the number of core clock cycles that is useful in measuring total execution time.

The performance counter can monitor either occurrence events or duration events. While counting occurrence events, the counter is incremented each time a specified event take place and while measuring duration, the counter counts the number of processor clocks that occur if a specified condition is true. If any of the 5 counters overflow, an interrupt request occurs when enabled. Each counter has its own interrupt request enable and continues to monitor events even after an overflow occurs until disabled by software.

For various events these counters can be programmed to refer to *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

3.2.12 Debug Unit

The debug unit is accessed through the JTAG port. The industry-standard, IEEE 1149.1 JTAG port consists of a test access port (TAP) controller, boundary-scan register, instruction and data registers, and dedicated signals TDI, TDO, TCK, TMS, and TRST_N.

The debug unit when used with debugger application code running on a host system outside of the Intel XScale processor allows a program, running on the Intel XScale processor, to be debugged. It allows the debugger application code or a debug exception to stop program execution and redirect execution to a debug-handling routine.

Debug exceptions are instruction breakpoint, data breakpoint, software breakpoint, external debug breakpoint, exception vector trap, trace buffer full breakpoint and SOC debug break. When a debug exception occurs, the processor's actions depend on whether the unit is configured for a halt mode or monitor mode.

When configured for Halt mode, the reset vector is overloaded to serve as the debug vector. A new processor mode called DEBUG mode, is added to allow handling of debug exceptions similar to other types of ARM exceptions. When a debug exceptions occurs, the processor switches to debug mode and redirects execution to a debug handler through reset vector. After the debug handler begins execution, the debugger can communicate with the debug handler to examine or alter processor state or memory through the JTAG interface.

When configured in Monitor mode, debug exceptions are handled like ARM prefetch aborts or ARM data aborts depending on the cause of the exception. When a debug exception occurs, the processor switches to abort mode and branches to a debug handler using the pre-fetch abort vector or data abort vector. The debugger then communicates with the debug handler to access processor state or memory contents.

The debug unit has two hardware-instruction, break point registers; two hardware, data-breakpoint registers; and a hardware, data-breakpoint control register. The second data-breakpoint register can be alternatively used as a mask register for the first data-breakpoint register.

A 256-entry trace buffer provides the ability to capture control flow messages or addresses. A JTAG instruction (LDIC) can be used to download a debug handler through the JTAG port to the mini-instruction cache. The I-cache has a 2-Kbyte, mini-instruction cache, like the mini-data cache, that is used only to hold a debug handler.

4.0 Package Information

The IXP43X network processors are built using a 460-ball, plastic ball grid array (PBGA) package.

4.1 Functional Signal Definitions

The signal definition tables list pull-up and pull-down resistor recommendations when a particular enabled interface is not being used in the application. These external resistor requirements are required only when a particular model of the Intel® IXP43X Product Line of Network Processor has a particular interface enabled and the interface is not required in the application.

Warning: With the exception of USB_V5REF all other I/O pins of the IXP43X network processors are not 5.0-V tolerant.

Disabled features within IXP43X network processors do not require external resistors as the processor has internal pull-up or pull-down resistors enabled as part of the **disabled** interface.

Table 9 presents the legend for interpreting the values in **Type** field that is referred in other tables in this section. To determine the disabled interfaces in the IXP43X network processors, refer to Table 1 on page 12.

4.1.1 Pin Types

Table 9. Signal Type Definitions (Sheet 1 of 2)

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
1	Driven to Vcc
0	Driven to Vss
X	Driven to unknown state
ID	Input is disabled
H	Pulled up to Vcc
L	Pulled to Vss
PD	Pull-up Disabled
Z	Output Disabled
VO	A valid output level is driven, allowed states -- 1, 0, H

Table 9. Signal Type Definitions (Sheet 2 of 2)

Symbol	Description
VB	Valid level on the signal, allowed states - 1, 0, H, Z
VI	Need to drive a valid input level, allowed states - 1, 0, H, Z
VOD	Valid Open Drain output, allowed states are 0 or Z
PE	Pull-up Enabled, equivalent to H
TRI	Output Only/Tristatable
N/C	No Connect
-	Pin is connected as described

4.1.2 Pin Description Tables

This section identifies all the signal pins by symbol name, type and description. Names should follow the following convention, all capital letters with a trailing "_N" indicate a signal is asserted when driven to a logic low (digital 0). The description includes the full name of the pin along with a functional description. This section does not specify the number of power and ground pins required, but does include the number of different types of power pins required.

A signal called active high specifies that the interface is active when driven to a logic 1 and inactive when driven to a logic 0.

A signal called active low specifies that the interface is active when driven to a logic 0 and inactive when driven to a logic 1.

The following information attempts to explain how to interpret the tables. There are five vertical columns:

- Power On Reset Active - This is when the Power on Reset signal is driven to logic 0. When this happens the part will behave as described in this column irrelevant of the settings on other signals.
- Reset Active - When Power on Reset is driven to a logic 1 and Reset is driven to a logic 0, the part will exhibit this behavior.
- Normal After Reset Until Software Enables - This is sometimes called safe mode. The intent of this is to allow the interface to be brought out of reset to a state, which will not cause any protocol violations or any damage to the parts prior to being enabled via software. This state will occur when both Power on Reset and Reset are driven to a logic 1.
- Possible Configurations after Software Enables - This state describes the way that the part is capable of behaving with appropriate software written. This state will occur when both Power on Reset and Reset are driven to a logic 1.

Table 10. Processors' Signal Interface Summary Table (Sheet 1 of 2)

Reference
Table 11, "DDRII/I SDRAM Interface" on page 39
Table 12, "PCI Controller" on page 41
Table 13, "High-Speed, Serial Interface 0" on page 44
Table 14, "UTOPIA Level 2/MII_A" on page 46
Table 15, "MII-C Interface" on page 51
Table 16, "Expansion Bus Interface" on page 52
Table 17, "UART Interface" on page 53
Table 18, "Serial Peripheral Port Interface" on page 54
Table 19, "USB Host" on page 55

Table 10. Processors' Signal Interface Summary Table (Sheet 2 of 2)

Reference
Table 20, "Oscillator Interface" on page 56
Table 21, "GPIO Interface" on page 56
Table 22, "JTAG Interface" on page 57
Table 23, "System Interface" on page 57
Table 24, "Power Interface" on page 58

Table 11. DDRII/I SDRAM Interface (Sheet 1 of 2)

Name	Power on Reset = 0 (has priority over Reset = 0)†	Reset=0 †	Normal After Reset Until Software Enables†	Possible Configurations After Software Enables†	Type†	Description
D_CK[2:0]/ DDR_CK[2:0]	X	X	VO	VO	O	DDRII/I SDRAM Clock Out — Provide positive differential clocks to the external SDRAM memory subsystem.
D_CK_N[2:0]/ DDR_CK_N[2:0]	X	X	VO	VO	O	DDRII/I SDRAM Clock Out — Provide negative differential clocks to the external SDRAM memory subsystem.
D_CS_N[1:0]/ DDR_CS_N[1:0]	b'11	b'11	VO	VO	O	Chip Select — To be asserted for all transactions to the DDRII/I SDRAM device. One per bank.
D_RAS_N/ DDR_RAS_N	1	1	VO	VO	O	Row Address Strobe — Indicates that the current address on D_MA[13:0]/DDR_MA[13:0] is the row.
D_CAS_N/ DDR_CAS_N	1	1	VO	VO	O	Column Address Strobe — Indicates that the current address on D_MA[13:0]/DDR_MA[13:0] is the column.
D_WE_N/ DDR_WE_N	1	1	VO	VO	O	Write Strobe — Defines whether or not the current operation by the DDRII/I SDRAM is to be a read or a write.
D_DM[4:0]/ DDR_DM[4:0]	Z	Z	VO	VO	O	Data Bus Mask — Controls the DDRII/1 SDRAM data input buffers. Asserting D_WE_N/ DDR_WE_N causes the data on D_DQ[31:0]/DDR_DQ[31:0] and D_CB[7:0]/DDR_CB[7:0] to be written into the DDRII/I SDRAM devices. D_DM[4:0]/DDR_DM[4:0] controls this operation on a per byte basis. D_DM[3:0]/DDR_DM[3:0] are intended to correspond to each byte of a word of data. D_DM[4]/DDR_DM[4] is intended to be utilized for the ECC byte of data.
D_BA[1:0]/ DDR_BA[1:0]	b'00	b'00	VO	VO	O	DDR SDRAM Bank Selects — Controls the internal DDR SDRAM Banks that are used to read or write. D_BA[1:0]/DDR_BA[1:0] are used for all technology types supported.
D_MA[13:0]/ DDR_MA[13:0]	0	0	VO	VO	O	Address bits 13 through 0 — Indicates the row or column to access depending on the state of D_RAS_N/DDR_RAS_N and D_CAS_N/DDR_CAS_N.
D_DQ[31:0]/ DDR_DQ[31:0]	Z	Z	VB	VB	I/O	Data Bus — 32-bit wide data bus.
D_CB[7:0]/ DDR_CB[7:0]	Z	Z	VB	VB	I/O	ECC Bus — Eight-bit error correction code that accompanies the data on D_DQ[31:0]/ DDR_DQ[31:0].
D_DQS[4:0]/ DDR_DQS[4:0]	Z	Z	VB	VB	I/O	Data Strobes Differential — Strobes that accompany the data to be read or written from the DDR SDRAM devices. Data is sampled on the negative and positive edges of these strobes. D_DQS[3:0]/DDR_DQS[3:0] are intended to correspond to each byte of a word of data. D_DQS[4]/DDR_DQS[4] is intended to be utilized for the ECC byte of data.
D_CKE[1:0]/ DDR_CKE[1:0]	b'00	b'00	VO	VO	O	Clock enables One clock after D_CKE[1:0]/DDR_CKE[1:0] is de-asserted, data is latched on D_DQ[31:0]/DDR_DQ[31:0] and D_CB[7:0]/DDR_CB[7:0]. Burst counters within DDR SDRAM device are not incremented. De-asserting this signal places the DDR SDRAM in self-refresh mode. For normal operation, D_CKE/DDR_CKE[1:0] to be asserted.

† Refer Table 9 on page 36 for legends of various **Type** codes

Table 11. DDRII/I SDRAM Interface (Sheet 2 of 2)

Name	Power on Reset = 0 (has priority over Reset = 0)†	Reset=0 †	Normal After Reset Until Software Enables†	Possible Configurations After Software Enables†	Type†	Description
D_DQS_N[4:0]	Z	Z	VB	VB	I/O	Complementary Data Strobes Differential: Differential pair signalling to the system during read and write.
D_VREF/DDR_VREF	VCCDDR/2	VCCDDR/2	VCCDDR/2	VCCDDR/2	I	DDR SDRAM Voltage Reference is used to supply the reference voltage to the differential inputs of the memory controller pins.
D_ODT[1:0]	Z	Z	VO	VO	O	On Die Termination Control — Turns on SDRAM termination during writes.
D_RES[2:1]	Z	Z	VB	VB	I/O	Compensation for DDR OCD (analog) DDRII mode only. This function is not enable and special connection is required. Refer to Figure 14.
D_SLWCRES	Z	Z	VB	VB	I/O	Compensation Voltage Reference (analog) for DDR driver slew rate control connected through a resistor to D_CRES0. Refer to Figure 13.
D_IMPCRES	Z	Z	VB	VB	I/O	Compensation Voltage Reference (analog) for DDR driver impedance control connected through a resistor to D_CRES0. Refer to Figure 13.
D_CRES0	Z	Z	VO	VO	O	Analog VSS Ref Pin (analog) both D_SLWCRES and D_IMPCRES signals connect to this pin through a reference resistor. Refer to Figure 13.
D_NC[4:0]	N/A	N/A	N/A	N/A	N/A	Reserved Pins for future use.

† Refer Table 9 on page 36 for legends of various **Type** codes

Table 12. PCI Controller (Sheet 1 of 3)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
PCI_AD[31:0]	Z	Z	VB	VB	I/O	PCI Address/Data bus is used to transfer address and bidirectional data to and from multiple PCI devices. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_CBE_N[3:0]	Z	Z	VB	VB	I/O	PCI Command/Byte Enables is used as a command word during PCI address cycles and as byte enables for data cycles. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_PAR	Z	Z	VB	VB	I/O	PCI Parity is used to check parity across the 32 bits of PCI_AD and the four bits of PCI_CBE_N. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_FRAME_N	Z	Z	VB	VB	I/O	PCI Cycle Frame is used to signify the beginning and duration of a transaction. The signal is inactive prior to or during the final data phase of a given transaction. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
PCI_TRDY_N	Z	Z	VB	VB	I/O	PCI Target Ready informs that the target of the PCI bus is ready to complete the current data phase of a given transaction. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_IRDY_N	Z	Z	VB	VB	I/O	PCI Initiator Ready informs the PCI bus that the initiator is ready to complete the transaction. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 12. PCI Controller (Sheet 2 of 3)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
PCI_STOP_N	Z	Z	VB	VB	I/O	PCI Stop indicates that the current target is requesting the current initiator to stop the current transaction. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_PERR_N	Z	Z	VB	VB	I/O	PCI Parity Error asserted when a PCI parity error is detected between the PCI_PAR and associated information on the PCI_AD bus and PCI_CBE_N during all PCI transactions, except for Special Cycles. The agent receiving data drives this signal. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_SERR_N	Z	Z	VB	VB	I/OD	PCI System Error asserted when a parity error occurs on special cycles or any other error that causes the PCI bus not to function properly. This signal can function as an input or an open drain output. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_DEVSEL_N	Z	Z	VB	VB	I/O	PCI Device Select: • When used as an output, PCI_DEVSEL_N indicates that device has decoded that address as the target of the requested transaction. • When used as an input, PCI_DEVSEL_N indicates if any device on the PCI bus exists with the given address. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_IDSEL	Z	Z	VI	VI	I	PCI Initialization Device Select is a chip select during configuration reads and writes. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 12. PCI Controller (Sheet 3 of 3)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
PCI_REQ_N[3:1]	Z	Z	VI	VI	I	PCI arbitration request: Used by the internal PCI arbiter to allow an agent to request the PCI bus. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_REQ_N[0]	Z	Z	VI	VI / VO	I/O	PCI arbitration request: • When configured as an input (PCI arbiter enabled), the internal PCI arbiter allows an agent to request the PCI bus. • When configured as an output (PCI arbiter disabled), the pin is used to request access to the PCI bus from an external arbiter. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_GNT_N[3:1]	Z	Z	VO	VO	O	PCI arbitration grant: It is generated by the internal PCI arbiter to allow an agent to claim control of the PCI bus.
PCI_GNT_N[0]	Z	Z	VO	VI / VO	I/O	PCI arbitration grant: • When configured as an output (PCI arbiter enabled), the internal PCI arbiter to allow an agent to claim control of the PCI bus. • When configured as an input (PCI arbiter disabled), the pin is used to claim access of the PCI bus from an external arbiter. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_INTA_N	Z	Z	Z	VOD	O/D	PCI interrupt: Used to request an interrupt. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the PCI soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
PCI_CLKIN	Z	VI	VI	VI	I	PCI Clock: This clock provides timing for all transactions on PCI. All PCI signals except INTA_N, INTB_N, INTC_N, and INTD_N are sampled on the rising edge of CLK and timing parameters are defined with respect to this edge. The PCI clock rate can operate at up to 33 MHz. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 13. High-Speed, Serial Interface 0

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
HSS_TXFRAME0	Z	Z	VB	VB	I/O	The High-Speed Serial (HSS) transmit frame signal can be configured either as an input or output to allow an external source to synchronize with the transmitted data. This is also known as Frame Sync signal and it is configured as an input upon reset. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the HSS soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
HSS_TXDATA0	Z	Z	VOD	VOD	OD	Transmit data out. Open Drain output. When this interface/signal is enabled, (though used or not used in a system design), the interface/signal should be pulled high with a 10-KΩ resistor to V_{CC33}. When this interface is disabled through the HSS soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
HSS_TXCLK0	Z	Z	VB	VB	I/O	The High-Speed Serial (HSS) transmit clock signal can be configured either as an input or an output. The clock can be of frequency ranging from 512 KHz to 8.192 MHz. Used to clock out the transmitted data. Configured as an input upon reset. Frame sync and Data can be selected to be generated on the rising or falling edge of the transmit clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
HSS_RXFRAME0	Z	Z	VB	VB	I/O	The High-Speed Serial (HSS) receive frame signal can be configured either as an input or an output to allow an external source to be synchronized with the received data. Often known as a Frame Sync signal. Configured as an input upon reset. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the HSS soft fuse (refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)* and is not being used in a system design, it is not required for any connection.

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 13. High-Speed, Serial Interface 0

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
HSS_RXDATA0	Z	VI	VI	VI	I	Receive data input. Can be sampled on the rising or falling edge of the receive clock. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the HSS soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
HSS_RXCLK0	Z	Z	VB	VB	I/O	The High-Speed Serial (HSS) receive clock signal can be configured as an input or an output. The clock can be from 512 KHz to 8.192 MHz. Used to sample the received data. Configured as an input upon reset. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 14. UTOPIA Level 2/MII_A (Sheet 1 of 5)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
UTP_OP_CLK / ETHA_TXCLK	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 Transmit clock input. Also known as UTP_TX_CLK. This signal is used to synchronize all UTOPIA Level 2 transmit output to the rising edge of the UTP_OP_CLK. MII Mode of Operation: Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
UTP_OP_FCO	Z	Z	Z	VO	TRI	UTOPIA Level 2 flow control output signal. Also known as the TXENB_N signal. Used to inform the selected PHY about data transmission. Placing the PHY's address on the UTP_OP_ADDR and bringing UTP_OP_FCO to logic 1 during the current clock, followed by the UTP_OP_FCO going to a logic 0, on the next clock cycle, selects the PHY that is active in MPHY mode. In SPHY configurations, UTP_OP_FCO is used to inform the PHY that the processor is ready to send data. This signal is tied to Vcc with an external 10-KΩ resistor.
UTP_OP_SOC	Z	Z	Z	VO	TRI	Start of Cell. Also known as TX_SOC. Active high signal is asserted when UTP_OP_DATA contains first valid byte of a transmitted cell. This signal is tied to Vss with an external 10-KΩ resistor.
UTP_OP_DATA[3:0] / ETHA_TXDATA[3:0]	Z	Z	Z	VO	TRI	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Transmit data bus to PHY, asserted synchronously with respect to ETHA_TXCLK. This MAC interface does not contain hardware hashing capabilities that are local to the interface. In this mode of operation the pins represented by this interface are ETHA_TXDATA[3:0].
UTP_OP_DATA[4] / ETHA_TXEN	Z	Z	Z	VO	TRI	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously, with respect to ETHA_TXCLK, at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC does not contain hardware hashing capabilities that are local to the interface.

† Refer Table 9 on page 36 for legends of various **Type** codes.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 14. UTOPIA Level 2/MII_A (Sheet 2 of 5)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
UTP_OP_DATA[7:5]	Z	Z	Z	VO	TRI	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 output data. Also known as UTP_TX_DATA. Used to send data from the processor to an ATM UTOPIA Level 2-compliant PHY.
UTP_OP_ADDR[4:0]	Z	Z	Z	VO	I/O	Transmit PHY address bus. Used by the processor when operating in MPHY mode to poll and select a single PHY at any given time. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_OP_FCI	Z	VI	VI	VI	I	UTOPIA Level 2 Output data flow control input: Also known as the TXFULL/CLAV signal. Used to inform the processor, the ability of each polled PHY to receive a complete cell. For cell-level flow control in an MPHY environment, TxClav is an active high tri-stateable signal from the MPHY to ATM layer. The UTP_OP_FCI is connected to multiple MPHY devices. It sees the logic high generated by the PHY, one clock after the given PHY address is asserted and a full cell can be received by the PHY. The UTP_OP_FCI sees a logic low generated by the PHY one clock cycle, after the PHY address is asserted, and a full cell cannot be received by the PHY. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
UTP_IP_CLK / ETHA_RXCLK	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 Receive clock input. Also known as UTP_RX_CLK. This signal is used to synchronize all UTOPIA Level 2-received inputs to the rising edge of the UTP_IP_CLK. MII Mode of Operation: Externally supplied receive clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC interface does not contain hardware hashing capabilities that are local to the interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

† Refer Table 9 on page 36 for legends of various **Type** codes.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 14. UTOPIA Level 2/MII_A (Sheet 3 of 5)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
UTP_IP_FCI	Z	VI	VI	VI	I	UTOPIA Level 2 Input Data flow control input signal. Also known as RXEMPTY/CLAV. Used to inform the processor of the ability of each polled PHY to send a complete cell. For cell-level flow control in an MPHY environment, RxClav is an active high tri-stateable signal from the MPHY to ATM layer. The UTP_IP_FCI, which is connected to multiple MPHY devices, sees logic high generated by the PHY, one clock after the given PHY address is asserted, when a full cell can be received by the PHY. The UTP_IP_FCI sees a logic low generated by the PHY, one clock cycle after the PHY address is asserted if a full cell cannot be received by the PHY. In a SPHY mode, this signal is used to indicate to the processor that the PHY has an octet or cell available for transferring to the processor. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse (refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)* and is not being used in a system design, the interface/signal is not required for any connection.
UTP_IP_SOC	Z	VI	VI	VI	I	Start of Cell. RX_SOC Active-high signal that is asserted when UTP_IP_DATA contains the first valid byte of a transmitted cell. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.
UTP_IP_DATA[3:0] / ETHA_RXDATA[3:0]	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Receives data bus from the PHY; asserted synchronously with respect to ETHA_RXCLK. When the interface/signal is enabled and is not being used in a system design, it should be pulled high with a 10KΩ resistor. When the interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. (Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)*.

† Refer Table 9 on page 36 for legends of various **Type** codes.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 14. UTOPIA Level 2/MII_A (Sheet 4 of 5)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
UTP_IP_DATA[4] / ETHA_RXDV	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by to the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Receive data valid used to inform the MII interface about data that is being sent by the Ethernet PHY. This MAC does not contain hardware hashing capabilities that are local to the interface. When the interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse (and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.
UTP_IP_DATA[5] / ETHA_COL	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. • When an NPE A is configured in UTOPIA Level 2 mode of operation and the signal is not used, it should be pulled high through a 10-KΩ resistor. MII Mode of Operation: Asserted by the PHY when a collision is detected by the PHY. • When an NPE A is configured in MII mode of operation and the signal is not used, it should be pulled low through a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/ or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

† Refer Table 9 on page 36 for legends of various **Type** codes.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 14. UTOPIA Level 2/MII_A (Sheet 5 of 5)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
UTP_IP_DATA[6] / ETHA_CRS	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Asserted by the PHY when transmit medium or receive medium is active. De-asserted when both the transmit and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETHA_RXCLK. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.
UTP_IP_DATA[7]	Z	VI	VI	VI	I	UTOPIA Level 2 Mode of Operation: UTOPIA Level 2 input data. Also known as RX_DATA. Used by the processor to receive data from an ATM UTOPIA Level 2-compliant PHY. MII Mode of Operation: Not Used. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor. When this interface is disabled through the UTOPIA Level 2 and/or the NPE-A Ethernet soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.
UTP_IP_ADDR[4:0]	Z	Z	Z	VO	I/O	Receive PHY address bus. Used by the processor while operating in an MPHY mode to poll and select a single PHY at any given point of time.
UTP_IP_FCO	Z	Z	Z	VO	TRI	UTOPIA Level 2 Input Data Flow Control Output signal: Also known as the RX_ENB_N. In a SPHY configuration, UTP_IP_FCO is used to inform the PHY that the processor is ready to accept data. In MPHY configurations, UTP_IP_FCO is used to select those PHY drives that signals UTP_RX_DATA and UTP_RX_SOC. The PHY is selected by placing the PHY's address on the UTP_IP_ADDR and bringing UTP_OP_FCO to logic 1 during the current clock, followed by the UTP_OP_FCO going to a logic 0 on the next clock cycle. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.

† Refer Table 9 on page 36 for legends of various **Type** codes.
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 15. MII-C Interface (Sheet 1 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
ETHC_MDIO	Z	Z	Z	VB	I/O	Management data input output. Provides the write data to both PHY devices connected to each MII interface. **An external pull-up resistor of 1.5K ohm is required on ETHC_MDIO to properly quantify the external PHYs used in the system.** For specific implementation, see the IEEE 802.3 specification. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_MDC	Z	Z	VI	VB	I/O	Management data clock. Management data interface clock is used to clock the MDIO signal as an output and sample the MDIO as an input. The ETHC_MDC is an input on power up and can be configured to be an output through Intel APIs documented in the *Intel® IXP400 Software Programmer's Guide*.
ETHC_txclk	Z	VI	VI	VI	I	Externally supplied transmit clock. • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities that are local to the interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled high with a 10-KΩ resistor.
ETHC_txdATA[3:0]	Z	0	VO	VO	O	Transmit data bus to PHY, asserted synchronously with respect to ETHC_TXCLK. This MAC contains hardware hashing capabilities that are local to the interface.
ETHC_txen	Z	0	VO	VO	O	Indicates that the PHY is being presented with nibbles on the MII interface. Asserted synchronously, with respect to ETHC_TXCLK, at the first nibble of the preamble, and remains asserted until all the nibbles of a frame are presented. This MAC contains hardware hashing capabilities that are local to the interface.
ETHC_rxclk	Z	VI	VI	VI	I	Externally supplied receive clock: • 25 MHz for 100 Mbps operation • 2.5 MHz for 10 Mbps This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_rxdATA[3:0]	Z	VI	VI	VI	I	Receive data bus from PHY, data sampled synchronously, with respect to ETHC_RXCLK. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
ETHC_rxdv	Z	VI	VI	VI	I	Receive data valid is used to inform the MII interface about data that is being sent by the Ethernet PHY This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.

† Refer Table 9 on page 36 for legends of various **Type** codes
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 15. MII-C Interface (Sheet 2 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
ETHC_col	Z	VI	VI	VI	I	Asserted by the PHY when a collision is detected by the PHY. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system When this interface is disabled through the NPE-C Ethernet soft fuse (refer to the Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual)* and is not being used a system design, this interface/signal is not required for any connection.
ETHC_crs	Z	VI	VI	VI	I	Asserted by the PHY when the transmit medium or receive medium are active. De-asserted when both the transmit and receive medium are idle. Remains asserted throughout the duration of collision condition. PHY asserts CRS asynchronously and de-asserts synchronously with respect to ETHC_RXCLK. This MAC contains hardware hashing capabilities that are local to the interface. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.

† Refer Table 9 on page 36 for legends of various **Type** codes
†† Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for information on how to select an interface.

Table 16. Expansion Bus Interface (Sheet 1 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
EX_CLK	Z	VI	VI	VI	I	Input clock signal is used to sample all expansion interface input and clock all expansion interface output.
EX_ALE	H	H	VO	VO	TRI	Expansion bus Address-latch enable is used for multiplexed address/data bus access and as an address valid signal for Synchronous Intel devices.
EX_ADDR[23:0]	Z	H	VB	VB	I/O	Expansion-bus address is used as an output for data access over the expansion bus. It is also used as an input during reset to capture device configuration. These signals have a weak pull-up resistor attached internally. Based on the desired configuration, various address signals should be tied low to enable operation of the device in the desired mode. A 470 ohm pull down resistor is required to override these pull-up resistors. Note: Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for additional information on address strapping.
EX_WR_N	Z	H	VB	VB	O	Expansion bus write enable signal

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 16. Expansion Bus Interface (Sheet 2 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
EX_RD_N	Z	H	VB	VB	O	Expansion bus read enable signal.
EX_CS_N[3:0]	Z	H	VB	VB	O	Used to drive chip selects for outbound transactions of the expansion bus.
EX_DATA[15:0]	Z	H	VB	VB	I/O	Expansion-bus, bidirectional data.
EX_IOWAIT_N	Z	VI	VI	VI	I	Data that is ready/acknowledge from expansion-bus devices. Expansion-bus access is halted when an external device sets EX_IOWAIT_N to logic 0 and resume from the halted location once the external device sets EX_IOWAIT_N to logic 1. This signal affects those access that use EX_CS_N[3:0] when the chip select is configured in Intel and Motorola* modes of operation. During idle cycles, the board is responsible for ensuring that EX_IOWAIT_N is pulled-up. It should be pulled high through a 10-KΩ resistor when it is not utilized in the system.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 17. UART Interface

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
RXDATA0	Z	VI	VI	VI	I	UART serial data input to UART Pins. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
TXDATA0	Z	V0	VO	VO	O	UART serial data output. The TXD signal is set to the MARKING (logic 1) state upon a reset operation.
CTS0_N	H	VI/H	VI/H	VI/H	I	UART CLEAR-TO-SEND input to UART Pins. When logic 0, this pin indicates that the modem or data set connected to the UART interface of the processor is ready to exchange data. The signal is a modem status input whose condition can be tested by the processor. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
RTS0_N	Z	V0	VO	VO	O	UART REQUEST-TO-SEND output: When logic 0, this informs the modem or the data set connected to the UART interface of the processor that the UART is ready to exchange data. A reset sets the request to send signal to logic 1. LOOP-mode operation holds this signal in its inactive state (logic 1).
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 18. Serial Peripheral Port Interface

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
SSP_SCLK	Z	0	VO	VO	O	SSP_SCLK is the serial bit clock used to control the timing of a transfer. SSP_SCLK can be generated internally (Master mode) as defined by a control register bit internal to IXP43X network processors.
SSP_SFRM	Z	1	VO	VO	O	SSP_SFRM is the serial frame indicator that indicates beginning and end of a serialized data word. The SSP_SFRM can be generated internally (Master mode) or taken from an external source (Slave mode) as defined by a control register bit internal to the IXP43X network processors. This signal is either active low or active high depending upon the mode of operation. Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for additional information.
SSP_TXD	Z	0	VO	VO	O	SSP_TXD is the Transmit data (serial data out) serialized data line. Sample length is a function of the selected serial data sample size.
SSP_RXD	Z	VI	VI	VI	I	SSP_RXD is the Receive data (serial data) in a serialized data line. Sample length is a function of the selected serial data sample size. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.
SSP_EXTCLK	Z	VI	VI	VI	I	SSP_EXTCLK is an external clock that can be selected to replace the internal 3.6864 MHz clock. The SSP_EXTCLK input is selected by setting various internal registers to appropriate values. Should be pulled high through a 10-KΩ resistor when not being utilized in the system.

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 19. USB Host

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
USB_P0_POS	Z	Z	VB	VB	I/O	Positive signal of the differential USB receiver/driver for the USB host interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P0_NEG	Z	Z	VB	VB	I/O	Negative signal of the differential USB receiver/driver for the USB host interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P0_PWREN	Z	Z	VO	VO	O	Enables the external VBUS power source.
USB_P0_OC	Z	Z	VI	VI	I	External VBUS power is in over current condition When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_POS	Z	Z	VB	VB	I/O	Positive signal of the differential USB receiver/driver for the USB host interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_NEG	Z	Z	VB	VB	I/O	Negative signal of the differential USB receiver/driver for the USB host interface. When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*
USB_P1_PWREN	Z	Z	VO	VO	O	Enable the external VBUS power source.
USB_P1_OC	Z	Z	VI	VI	I	External VBUS power is in over current condition When this interface/signal is enabled and is not being used in a system design, the interface/signal should be pulled low with a 10-KΩ resistor. When this interface is disabled through the USB Device soft fuse and is not being used in a system design, it is not required for any connection. Refer to Expansion Bus Controller chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual.*

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 20. Oscillator Interface

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
OSC_IN	n/a	VI	VI	VI	I	33.33-MHz, sinusoidal input signal. Can be driven by an oscillator.
OSC_OUT	n/a	VO	VO	VO	O	33.33-MHz, sinusoidal output signal. Left disconnected when being driven by an oscillator.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 21. GPIO Interface

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
GPIO[12:0]	Z	Z	VI	VB	I/O	General purpose Input/Output pins. Can be configured as an input or an output. As an input, each signal can be configured a processor interrupt. Default after reset is to be configured as input. Some GPIO may serve as an optional alternate function. Refer to Section 3.1.11, "GPIO" on page 27 for additional details on the alternate function mapping. Should be pulled high using a 10-KΩ resistor when it is not utilized in the system.
GPIO[13]	Z	Z	VI	VB	I/O	General purpose Input/Output pins. May be configured as an input or an output. Default after reset is to be configured as inputs. Some GPIO may serve as an optional alternate function. Refer to Section 3.1.11, "GPIO" on page 27 for additional details on the alternate function mapping. Should be pulled high using a 10-KΩ resistor when it is not utilized in the system.
GPIO[14]	Z	Z	VI	VB	I/O	Can be configured in the same as GPIO Pin 13 or a clock output. Configuration as an output clock can be set at various speeds up to 33.33 MHz with various duty cycles. Configured as an input upon reset. Some GPIO may serve as an optional alternate function. Refer to Section 3.1.11, "GPIO" on page 27 for additional details on the alternate function mapping. Should be pulled high through a 10-KΩ resistor when not utilized in the system.
GPIO[15]	0	clkout / VO	VO	VB	I/O	Can be configured the same as GPIO Pin [13:8] or as a clock output. Configuration as an output clock can be set at various speeds of up to 33.33 MHz with various duty cycles. As an input, signal can be configured as a processor interrupt for Type Register 2.Configured as an output upon reset. Can be used to clock the expansion interface after reset. Some GPIO may serve as an optional alternate function. Refer to Section 3.1.11, "GPIO" on page 27 for additional details on the alternate function mapping. Should be pulled high through a 10-KΩ resistor and is set to an input when it is not utilized in the system. The interface should be set to an input in when not used.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 22. JTAG Interface

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
JTG_TMS	H	VI / H	VI/H	VI/H	I	Test mode selected for the IEEE 1149.1 JTAG interface.
JTG_TDI	H	VI /H	VI/H	VI/H	I	Input data for the IEEE 1149.1 JTAG interface.
JTG_TDO	Z	VO/Z	VO / Z	VO / Z	TRI	Output data for the IEEE 1149.1 JTAG interface.
JTG_TRST_N	H	VI/H	VI	VI	I	Used to reset the IEEE 1149.1 JTAG interface. ***Note:*** The JTG_TRST_N signal should be asserted (driven low) during power-up, else the TAP controller will not be initialized properly and the processor can be locked. When the JTAG interface is not being used, the signal is pulled low using a 10-KΩ resistor.
JTG_TCK	Z	VI	VI	VI	I	Used as the clock for the IEEE 1149.1 JTAG interface.

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 23. System Interface (Sheet 1 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Normal After Software Enables	Type†	Description
BYPASS_CLK	Z	VI	VI	VI	I	Used for testing only. It is pulled high using a 10-KΩ resistor under normal operation.
SCANTESTMODE_N	VI/H	VI/H	VI / H	VI / H	I	Used for testing only. It is pulled high using a 10-KΩ resistor under normal operation.
RESET_IN_N	VI/H	VI/H	VI / H	VI / H	I	Used as a reset input to the device when PWRON_RESET_N is in an inactive state and once power up conditions are met. Power up conditions include the following: 1. Power supplies reaching a safe stable condition and 2. The PLL achieving a locked state
PWRON_RESET_N	VI/H	VI/H	V I/ H	VI / H	I	Signal that is used reset all internal logic to a known state. The PWRON_RESET_N signal is a 3.3-V signal.
HIGHZ_N	VI / H	VI / H	VI / H	VI / H	I	Used for testing only Is pulled high using a 10-KΩ resistor for normal operation.
USB_RBIASP	Z	VO	VO	VO	O	Analog pin is used for RCOMP and iCOMP® and must be connected to a 22.6Ω resistor to ground. Refer to Figure 15.

† Refer Table 9 on page 36 for legends of various **Type** codes.

Table 23. System Interface (Sheet 2 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Normal After Software Enables	Type†	Description
USB_RBIASN	Z	Z	VI	VI	I	Analog pin shorted to USB_RBIASP to provide feedback to internal circuitry for RCOMP and ICOMP. Refer to Figure 15.
PLL_LOCK	0	VO	VO	VO	O	Signal used to inform an external reset logic about achievement of locked state by internal PLL. PLL_LOCK is de-asserted during a watchdog timeout.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 24. Power Interface (Sheet 1 of 2)

Name	Power on Reset†	Reset†	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
VCC	N/A	N/A	N/A	N/A	I	1.3-V power supply input pins are used for the internal logic.
VCC33	N/A	N/A	N/A	N/A	I	3.3-V power supply input pins are used for the peripheral (I/O) logic.
VCCDDR	N/A	N/A	N/A	N/A	I	1.8-V or 2.5-V power supply input pins are used for the DDR memory interface.
VSS	N/A	N/A	N/A	N/A	I	Ground power supply input pins are used for the 3.3-V, 2.5-V, 1.8-V, and the 1.3-V power supplies.
USB_v5REF	N/A	N/A	N/A	N/A	I	5-V power supply input pins are used for reference voltage. **Note:** 3.3-V power supply input can be used but causes damage to the USB controller if signal pin is shorted to 5V VBUS.
VCCP_OSC	N/A	N/A	N/A	N/A	I	3.3-V power supply input pins are used for peripheral (I/O) logic of the analog oscillator circuitry. Require special power filtering circuitry. Refer to Figure 10 on page 88.
VCCF	N/A	N/A	N/A	N/A	I	1.3-V power supply input pin. Dedicated for Fuse.
VSSAUBG	N/A	N/A	N/A	N/A	I	Specialized ground for USB Band Gap.
VCCAUPLL	N/A	N/A	N/A	N/A	I	1.3-V power supply input pins are used for USB PLL. Requires special power filtering circuitry. Refer to Figure 11 on page 88.
VCCAUBG	N/A	N/A	N/A	N/A	I	3.3-V power supply input pins are used for USB Band Gap Requires special power filtering circuitry. Refer to Figure 12 on page 89.
VCCPUSB	N/A	N/A	N/A	N/A	I	3.3-V power supply input pins are used for USB IO.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

Table 24. Power Interface (Sheet 2 of 2)

Name	Power on Reset†	Reset †	Normal After Reset Until Software Enables	Possible Configurations After Software Enables	Type†	Description
VCCUSBCORE	N/A	N/A	N/A	N/A	I	1.3-V power supply input pins are used for USB IO core.
VCCA	N/A	N/A	N/A	N/A	I	1.3-V power supply input pins are used for internal logic of the analog phase lock-loop circuitry. Requires special power filtering circuitry. Refer to Figure 9 on page 87.
† Refer Table 9 on page 36 for legends of various **Type** codes.						

4.2 Package Description

The package is shown in Figure 7 and Figure 8.

Figure 7. 460-Pin PBGA Package (Side View)

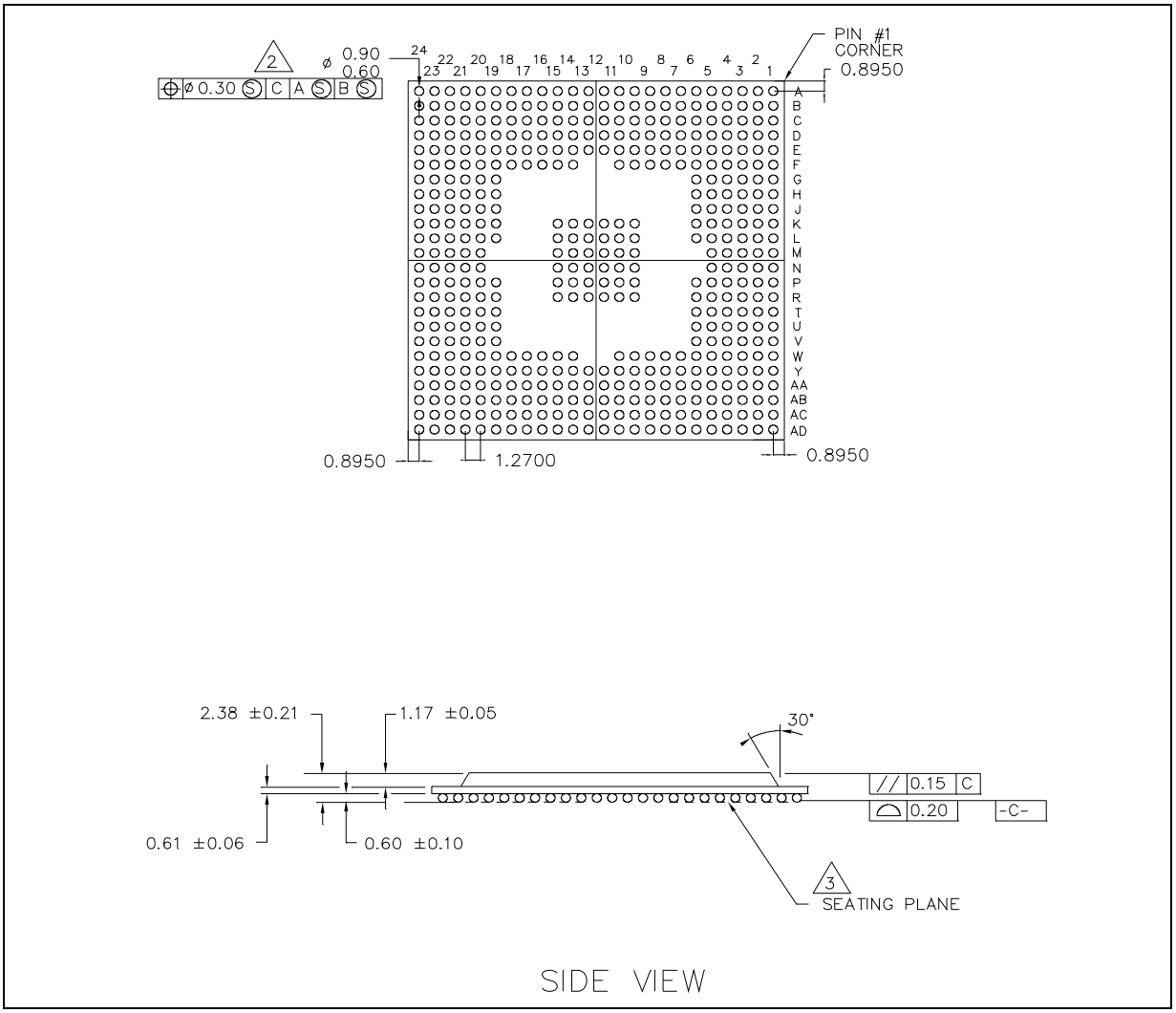


Figure 8. 460-Pin PBGA Package (Top and Bottom View)

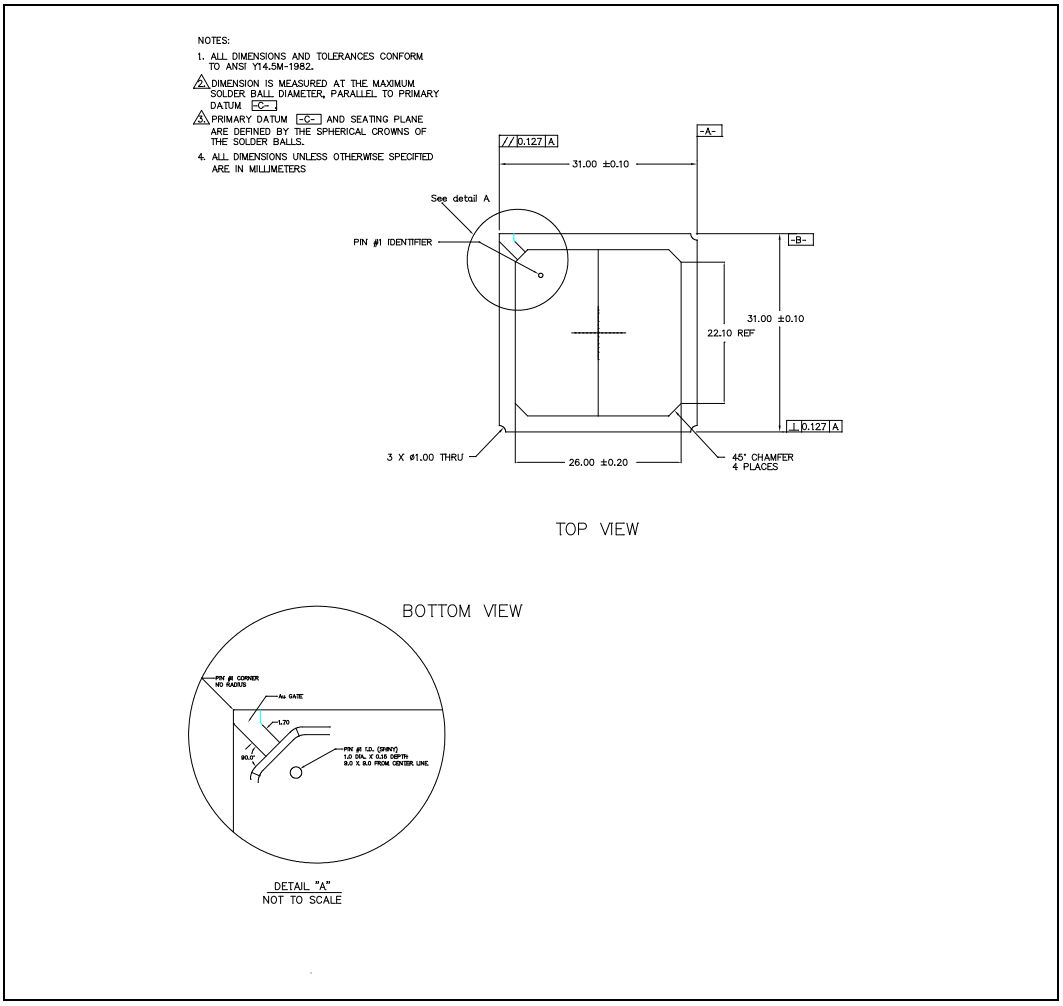


Table 25. Part Numbers; Lead Free (pb-free) Packaging

Device	Stepping	Speed (MHz)	Part Number	Temperature Offering
Intel® IXP435 Network Processor	A1	667	NHIXP435AE	Commercial
Intel® IXP435 Network Processor	A1	667	NHIXP435AET	Extended
Intel® IXP435 Network Processor	A1	533	NHIXP435AD	Commercial
Intel® IXP435 Network Processor	A1	533	NHIXP435ADT	Extended
Intel® IXP435 Network Processor	A1	400	NHIXP435AC	Commercial
Intel® IXP435 Network Processor	A1	400	NHIXP435ACT	Extended
Intel® IXP433 Network Processor	A1	533	NHIXP433AD	Commercial
Intel® IXP432 Network Processor	A1	400	NHIXP432AC	Commercial
Intel® IXP431 Network Processor	A1	400	NHIXP431AC	Commercial
Intel® IXP430 Network Processor	A1	667	NHIXP430AE	Commercial

Table 25. Part Numbers; Lead Free (pb-free) Packaging

Device	Stepping	Speed (MHz)	Part Number	Temperature Offering
Intel® IXP430 Network Processor	A1	533	NHIXP430AD	Commercial
Intel® IXP430 Network Processor	A1	400	NHIXP430AC	Commercial
Intel® IXP430 Network Processor	A1	400	NHIXP430ACT	Extended

4.3 Signal-Pin Description

While designing with a multi-function processor, you can build a board design that allows a group of products to be produced from a single board design. When this occurs, some features of a given processor are not used.

Table 26. Processors' Ball Map Assignments (Sheet 1 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
A1	VSS		X	X	X	X	X
A2	VSS		X	X	X	X	X
A3	VCCDDR		X	X	X	X	X
A4	D_RES[2]		X	X	X	X	X
A5	D_MA[6]]		X	X	X	X	X
A6	D_WE_N		X	X	X	X	X
A7	VSS		X	X	X	X	X
A8	D_DQ[31]		X	X	X	X	X
A9	D_MA[13]		X	X	X	X	X
A10	D_MA[11]		X	X	X	X	X
A11	D_CB[4]		X	X	X	X	X
A12	D_CB[6]		X	X	X	X	X
A13	D_CB[3]		X	X	X	X	X
A14	D_CS_N[0]		X	X	X	X	X
A15	VSS		X	X	X	X	X
A16	USB_P1_NEG		X	X	X	X	X
A17	VSS		X	X	X	X	X
A18	USB_P0_NEG		X	X	X	X	X
A19	VCCAUBG		X	X	X	X	X
A20	USB_P0_PWREN		X	X	X	X	X
A21	PCI_REQ_N[3]		X	X	X	X	X
A22	PCI_AD[30]		X	X	X	X	X
A23	PCI_AD[24]		X	X	X	X	X
A24	VSS		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 2 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
B1	VSS		X	X	X	X	X
B2	VSS		X	X	X	X	X
B3	VCCDDR		X	X	X	X	X
B4	D_RES[1]		X	X	X	X	X
B5	VSS		X	X	X	X	X
B6	D_DQ[28]		X	X	X	X	X
B7	D_DQ[24]		X	X	X	X	X
B8	D_DQ[30]		X	X	X	X	X
B9	D_DQ[27]		X	X	X	X	X
B10	VCCDDR		X	X	X	X	X
B11	D_CB[1]		X	X	X	X	X
B12	D_DQS[4]		X	X	X	X	X
B13	D_CB[2]		X	X	X	X	X
B14	D_CKE[1]		X	X	X	X	X
B15	VCCDDR		X	X	X	X	X
B16	USB_P1_POS		X	X	X	X	X
B17	VSS		X	X	X	X	X
B18	USB_P0_POS		X	X	X	X	X
B19	VSSAUBG		X	X	X	X	X
B20	USB_P1_PWREN		X	X	X	X	X
B21	PCI_GNT_N[0]		X	X	X	X	X
B22	PCI_REQ_N[1]		X	X	X	X	X
B23	PCI_IDSEL		X	X	X	X	X
B24	PCI_AD[20]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 3 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
C1	VCCDDR		X	X	X	X	X
C2	VSS		X	X	X	X	X
C3	VSS		X	X	X	X	X
C4	D_CRES0		X	X	X	X	X
C5	D_BA[0]		X	X	X	X	X
C6	D_CK_N[2]		X	X	X	X	X
C7	D_DQ[25]		X	X	X	X	X
C8	D_DQS_N[3]		X	X	X	X	X
C9	D_DQ[26]		X	X	X	X	X
C10	D_CB[5]		X	X	X	X	X
C11	D_CB[0]		X	X	X	X	X
C12	D_DQS_N[4]		X	X	X	X	X
C13	D_CB[7]		X	X	X	X	X
C14	D_CKE[0]		X	X	X	X	X
C15	D_CS_N[1]		X	X	X	X	X
C16	VSS		X	X	X	X	X
C17	USB_RBIASP		X	X	X	X	X
C18	VSS		X	X	X	X	X
C19	USB_P0_OC		X	X	X	X	X
C20	PCI_SERR_N		X	X	X	X	X
C21	PCI_REQ_N[2]		X	X	X	X	X
C22	PCI_AD[27]		X	X	X	X	X
C23	PCI_AD[18]		X	X	X	X	X
C24	VCC33		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 4 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
D1	D_MA[5]		X	X	X	X	X
D2	VCCDDR		X	X	X	X	X
D3	D_DM[2]		X	X	X	X	X
D4	D_DQ[17]		X	X	X	X	X
D5	D_CK[0]		X	X	X	X	X
D6	D_CK[2]		X	X	X	X	X
D7	D_DQ[29]		X	X	X	X	X
D8	D_DQS[3]		X	X	X	X	X
D9	D_DM[3]		X	X	X	X	X
D10	D_MA[12]		X	X	X	X	X
D11	D_MA[10]		X	X	X	X	X
D12	VSS		X	X	X	X	X
D13	D_DM[4]		X	X	X	X	X
D14	VSS		X	X	X	X	X
D15	D_ODT[1]		X	X	X	X	X
D16	VCCDDR		X	X	X	X	X
D17	USB_RBIASN		X	X	X	X	X
D18	VSS		X	X	X	X	X
D19	USB_P1_OC		X	X	X	X	X
D20	PCI_GNT_N[3]		X	X	X	X	X
D21	PCI_AD[31]		X	X	X	X	X
D22	PCI_AD[21]		X	X	X	X	X
D23	PCI_AD[16]		X	X	X	X	X
D24	PCI_STOP_N		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 5 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
E1	D_RAS_N		X	X	X	X	X
E2	D_DQ[22]		X	X	X	X	X
E3	D_DQ[16]		X	X	X	X	X
E4	D_DQS[2]		X	X	X	X	X
E5	D_CK_N[0]		X	X	X	X	X
E6	D_BA[1]		X	X	X	X	X
E7	VCCDDR		X	X	X	X	X
E8	D_MA[7]		X	X	X	X	X
E9	D_ODT[0]		X	X	X	X	X
E10	VSS		X	X	X	X	X
E11	VCCDDR		X	X	X	X	X
E12	VCC		X	X	X	X	X
E13	VCC		X	X	X	X	X
E14	VCCDDR		X	X	X	X	X
E15	VCCDDR		X	X	X	X	X
E16	VCCPUSB		X	X	X	X	X
E17	VCCPUSB		X	X	X	X	X
E18	VCCUSBCORE		X	X	X	X	X
E19	VSS		X	X	X	X	X
E20	PCI_GNT_N[2]		X	X	X	X	X
E21	PCI_AD[28]		X	X	X	X	X
E22	VSS		X	X	X	X	X
E23	VCC33		X	X	X	X	X
E24	VSS		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 6 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
F1	VSS		X	X	X	X	X
F2	D_DQ[18]		X	X	X	X	X
F3	D_DQ[23]		X	X	X	X	X
F4	D_DQS_N[2]		X	X	X	X	X
F5	D_DQ[21]		X	X	X	X	X
F6	D_IMPCRES		X	X	X	X	X
F7	D_SLWCRES		X	X	X	X	X
F8	D_VREF		X	X	X	X	X
F9	VCC		X	X	X	X	X
F10	VCC		X	X	X	X	X
F11	VCC		X	X	X	X	X
F12							
F13							
F14	VCC		X	X	X	X	X
F15	VCC		X	X	X	X	X
F16	VCC		X	X	X	X	X
F17	USB_V5REF		X	X	X	X	X
F18	VCCUSBCORE		X	X	X	X	X
F19	VCCAUPLL		X	X	X	X	X
F20	PCI_REQ_N[0]		X	X	X	X	X
F21	PCI_CBE_N[3]		X	X	X	X	X
F22	PCI_CLKIN		X	X	X	X	X
F23	PCI_PERR_N		X	X	X	X	X
F24	PCI_AD[15]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 7 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
G1	D_DQ[1]		X	X	X	X	X
G2	D_DQ[4]		X	X	X	X	X
G3	D_DQ[5]		X	X	X	X	X
G4	D_DQ[19]		X	X	X	X	X
G5	D_DQ[20]		X	X	X	X	X
G6	VSS		X	X	X	X	X
G7							
G8							
G9							
G10							
G11							
G12							
G13							
G14							
G15							
G16							
G17							
G18							
G19	PCI_INTA_N		X	X	X	X	X
G20	PCI_AD[29]		X	X	X	X	X
G21	PCI_AD[25]		X	X	X	X	X
G22	PCI_IRDY_N		X	X	X	X	X
G23	PCI_AD[13]		X	X	X	X	X
G24	PCI_AD[12]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 8 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
H1	D_DM[0]		X	X	X	X	X
H2	D_DQ[0]		X	X	X	X	X
H3	D_DQS_N[0]		X	X	X	X	X
H4	D_CAS_N		X	X	X	X	X
H5	VSS		X	X	X	X	X
H6	VCCDDR		X	X	X	X	X
H7							
H8							
H9							
H10							
H11							
H12							
H13							
H14							
H15							
H16							
H17							
H18							
H19	PCI_GNT_N[1]		X	X	X	X	X
H20	VSS		X	X	X	X	X
H21	PCI_AD[23]		X	X	X	X	X
H22	PCI_CBE_N[2]		X	X	X	X	X
H23	VCC33		X	X	X	X	X
H24	PCI_CBE_N[0]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 9 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
J1	D_DQ[7]		X	X	X	X	X
J2	D_DQ[6]		X	X	X	X	X
J3	D_DQS[0]		X	X	X	X	X
J4	VCCDDR		X	X	X	X	X
J5	D_MA[4]		X	X	X	X	X
J6	VCC		X	X	X	X	X
J7							
J8							
J9							
J10							
J11							
J12							
J13							
J14							
J15							
J16							
J17							
J18							
J19	VCC		X	X	X	X	X
J20	PCI_AD[26]		X	X	X	X	X
J21	PCI_AD[19]		X	X	X	X	X
J22	PCI_PAR		X	X	X	X	X
J23	VSS		X	X	X	X	X
J24	PCI_AD[4]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 10 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
K1	D_DQ[3]		X	X	X	X	X
K2	D_DQ[2]		X	X	X	X	X
K3	VSS		X	X	X	X	X
K4	D_MA[3]		X	X	X	X	X
K5	D_MA[2]		X	X	X	X	X
K6	VCC		X	X	X	X	X
K7							
K8							
K9							
K10	VSS		X	X	X	X	X
K11	VSS		X	X	X	X	X
K12	VSS		X	X	X	X	X
K13	VSS		X	X	X	X	X
K14	VSS		X	X	X	X	X
K15	VSS		X	X	X	X	X
K16							
K17							
K18							
K19	VCC		X	X	X	X	X
K20	PCI_AD[22]		X	X	X	X	X
K21	PCI_FRAME_N		X	X	X	X	X
K22	PCI_CBE_N[1]		X	X	X	X	X
K23	PCI_AD[6]		X	X	X	X	X
K24	PCI_TRDY_N		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 11 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
L1	D_DQ[9]		X	X	X	X	X
L2	D_DQ[12]		X	X	X	X	X
L3	D_DQ[13]		X	X	X	X	X
L4	D_MA[1]		X	X	X	X	X
L5	D_MA[0]		X	X	X	X	X
L6	VCC		X	X	X	X	X
L7							
L8							
L9							
L10	VSS		X	X	X	X	X
L11	VSS		X	X	X	X	X
L12	VSS		X	X	X	X	X
L13	VSS		X	X	X	X	X
L14	VSS		X	X	X	X	X
L15	VSS		X	X	X	X	X
L16							
L17							
L18							
L19	VCC		X	X	X	X	X
L20	PCI_AD[17]		X	X	X	X	X
L21	PCI_DEVSEL_N		X	X	X	X	X
L22	PCI_AD[14]		X	X	X	X	X
L23	PCI_AD[8]		X	X	X	X	X
L24	PCI_AD[5]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 12 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
M1	D_DQ[8]		X	X	X	X	X
M2	VSS		X	X	X	X	X
M3	D_DQS[1]		X	X	X	X	X
M4	VCCDDR		X	X	X	X	X
M5	VCC		X	X	X	X	X
M6							
M7							
M8							
M9							
M10	VSS		X	X	X	X	X
M11	VSS		X	X	X	X	X
M12	VSS		X	X	X	X	X
M13	VSS		X	X	X	X	X
M14	VSS		X	X	X	X	X
M15	VSS		X	X	X	X	X
M16							
M17							
M18							
M19							
M20	VCC		X	X	X	X	X
M21	PCI_AD[11]		X	X	X	X	X
M22	PCI_AD[10]		X	X	X	X	X
M23	PCI_AD[3]		X	X	X	X	X
M24	VSS		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 13 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
N1	D_DQ[15]		X	X	X	X	X
N2	D_DQ[14]		X	X	X	X	X
N3	D_DQS_N[1]		X	X	X	X	X
N4	D_DM[1]		X	X	X	X	X
N5	VCC		X	X	X	X	X
N6							
N7							
N8							
N9							
N10	VSS		X	X	X	X	X
N11	VSS		X	X	X	X	X
N12	VSS		X	X	X	X	X
N13	VSS		X	X	X	X	X
N14	VSS		X	X	X	X	X
N15	VSS		X	X	X	X	X
N16							
N17							
N18							
N19							
N20	VCC		X	X	X	X	X
N21	PCI_AD[9]		X	X	X	X	X
N22	PCI_AD[2]		X	X	X	X	X
N23	VCC33		X	X	X	X	X
N24	SSP_SCLK		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 14 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
P1	D_DQ[10]		X	X	X	X	X
P2	VCCDDR		X	X	X	X	X
P3	D_DQ[11]		X	X	X	X	X
P4	VSS		X	X	X	X	X
P5	D_VREF		X	X	X	X	X
P6	VCC		X	X	X	X	X
P7							
P8							
P9							
P10	VSS		X	X	X	X	X
P11	VSS		X	X	X	X	X
P12	VSS		X	X	X	X	X
P13	VSS		X	X	X	X	X
P14	VSS		X	X	X	X	X
P15	VSS		X	X	X	X	X
P16							
P17							
P18							
P19	VCC		X	X	X	X	X
P20	PCI_AD[0]		X	X	X	X	X
P21	PCI_AD[7]		X	X	X	X	X
P22	PCI_AD[1]		X	X	X	X	X
P23	SSP_RXD		X	X	X	X	X
P24	SSP_EXTCLK		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 15 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
R1	D_CK_N[1]		X	X	X	X	X
R2	D_CK[1]		X	X	X	X	X
R3	D_MA[8]		X	X	X	X	X
R4	VCC33		X	X	X	X	X
R5	D_MA[9]		X	X	X	X	X
R6	VCC		X	X	X	X	X
R7							
R8							
R9							
R10	VSS		X	X	X	X	X
R11	VSS		X	X	X	X	X
R12	VSS		X	X	X	X	X
R13	VSS		X	X	X	X	X
R14	VSS		X	X	X	X	X
R15	VSS		X	X	X	X	X
R16							
R17							
R18							
R19	VCC		X	X	X	X	X
R20	SSP_SFRM		X	X	X	X	X
R21	SSP_TXD		X	X	X	X	X
R22	CTSO_N		X	X	X	X	X
R23	TXDATA0		X	X	X	X	X
R24	RTSO_N		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 16 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
T1	VSS		X	X	X	X	X
T2	HSS_TXFRAME0		X	X		X	
T3	HSS_TXDATA0		X	X		X	
T4	HSS_RXFRAME0		X	X		X	
T5	HSS_RXDATA0		X	X		X	
T6	VCC		X	X	X	X	X
T7							
T8							
T9							
T10							
T11							
T12							
T13							
T14							
T15							
T16							
T17							
T18							
T19	VCC		X	X	X	X	X
T20	GPIO[15]		X	X	X	X	X
T21	RXDATA0		X	X	X	X	X
T22	GPIO[11]		X	X	X	X	X
T23	GPIO[13]		X	X	X	X	X
T24	GPIO[14]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 17 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
U1	VCC33		X	X	X	X	X
U2	HSS_TXCLK0		X	X		X	
U3	HSS_RXCLK0		X	X		X	
U4	ETHC_TXDATA[2]		X	X	X	X	X
U5	ETHC_TXDATA[0]		X	X	X	X	X
U6	VSS		X	X	X	X	X
U7							
U8							
U9							
U10							
U11							
U12							
U13							
U14							
U15							
U16							
U17							
U18							
U19	GPIO[6]		X	X	X	X	X
U20	GPIO[7]		X	X	X	X	X
U21	GPIO[9]		X	X	X	X	X
U22	GPIO[10]		X	X	X	X	X
U23	GPIO[12]		X	X	X	X	X
U24	VSS		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 18 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
V1	ETHC_TXDATA[1]		X	X	X	X	X
V2	ETHC_TXDATA[3]		X	X	X	X	X
V3	ETHC_RXDV		X	X	X	X	X
V4	VCC33		X	X	X	X	X
V5	ETHC_RXDATA[0]		X	X	X	X	X
V6	VCC33		X	X	X	X	X
V7							
V8							
V9							
V10							
V11							
V12							
V13							
V14							
V15							
V16							
V17							
V18							
V19	VCCF		X	X	X	X	X
V20	GPIO[0]		X	X	X	X	X
V21	GPIO[4]		X	X	X	X	X
V22	GPIO[3]		X	X	X	X	X
V23	GPIO[5]		X	X	X	X	X
V24	GPIO[8]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 19 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
W1	ETHC_RXDATA[3]		X	X	X	X	X
W2	ETHC_TXCLK		X	X	X	X	X
W3	VSS		X	X	X	X	X
W4	ETHC_CRS		X	X	X	X	X
W5	ETHC_TXEN		X	X	X	X	X
W6	UTP_OP_DATA[7]		X			X	
W7	UTP_IP_DATA[5]	ETHA_COL	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
W8	UTP_IP_DATA[1]	ETHA_RXDATA[1]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
W9	VCC		X	X	X	X	X
W10	VCC		X	X	X	X	X
W11	VCC		X	X	X	X	X
W12							
W13							
W14	VCC		X	X	X	X	X
W15	VCC		X	X	X	X	X
W16	VCC		X	X	X	X	X
W17	EX_DATA[5]		X	X	X	X	X
W18	EX_ADDR[10]		X	X	X	X	X
W19	EX_ADDR[3]		X	X	X	X	X
W20	VCC33		X	X	X	X	X
W21	EX_ADDR[1]		X	X	X	X	X
W22	EX_ADDR[0]		X	X	X	X	X
W23	GPIO[1]		X	X	X	X	X
W24	GPIO[2]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 20 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
Y1	ETHC_RXDATA[1]		X	X	X	X	X
Y2	ETHC_RXDATA[2]		X	X	X	X	X
Y3	ETHC_RXCLK		X	X	X	X	X
Y4	ETHC_MDC		X	X	X	X	X
Y5	UTP_OP_DATA[4]	ETHA_TXEN	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
Y6	UTP_IP_DATA[6]	ETHA_CRS	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
Y7	VSS		X	X	X	X	X
Y8	UTP_OP_ADDR[4]		X			X	
Y9	UTP_IP_SOC		X			X	
Y10	UTP_IP_ADDR[2]		X			X	
Y11	VCC		X	X	X	X	X
Y12	VCC		X	X	X	X	X
Y13	VCC		X	X	X	X	X
Y14	VCCA		X	X	X	X	X
Y15	EX_ADDR[17]		X	X	X	X	X
Y16	EX_DATA[15]		X	X	X	X	X
Y17	EX_DATA[10]		X	X	X	X	X
Y18	EX_DATA[4]		X	X	X	X	X
Y19	EX_DATA[1]		X	X	X	X	X
Y20	EX_ADDR[9]		X	X	X	X	X
Y21	EX_ADDR[6]		X	X	X	X	X
Y22	EX_ADDR[4]		X	X	X	X	X
Y23	EX_ADDR[5]		X	X	X	X	X
Y24	EX_ADDR[2]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 21 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
AA1	ETHC_MDIO		X	X	X	X	X
AA2	ETHC_COL		X	X	X	X	X
AA3	UTP_OP_DATA[5]		X			X	
AA4	VSS		X	X	X	X	X
AA5	UTP_OP_DATA[0]	ETHA_TXDATA[0]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AA6	UTP_OP_FCO		X			X	
AA7	UTP_OP_CLK	ETHA_TXCLK	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AA8	UTP_OP_ADDR[0]		X			X	
AA9	UTP_IP_ADDR[4]		X			X	
AA10	UTP_IP_ADDR[0]		X			X	
AA11	SCANTESTMODE_N		X	X	X	X	X
AA12	VCCA		X	X	X	X	X
AA13	VCCA		X	X	X	X	X
AA14	VCCP_OSC		X	X	X	X	X
AA15	EX_ADDR[23]		X	X	X	X	X
AA16	EX_ADDR[16]		X	X	X	X	X
AA17	EX_ADDR[13]		X	X	X	X	X
AA18	EX_DATA[13]		X	X	X	X	X
AA19	EX_DATA[11]		X	X	X	X	X
AA20	EX_DATA[2]		X	X	X	X	X
AA21	EX_DATA[0]		X	X	X	X	X
AA22	EX_ADDR[11]		X	X	X	X	X
AA23	EX_ADDR[8]		X	X	X	X	X
AA24	EX_ADDR[7]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 22 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
AB1	VCC33		X	X	X	X	X
AB2	UTP_OP_DATA[6]		X			X	
AB3	UTP_OP_DATA[3]	ETHA_TXDATA[3]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AB4	UTP_IP_DATA[7]		X			X	
AB5	UTP_IP_DATA[2]	ETHA_RXDATA[2]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AB6	UTP_OP_FCI		X			X	
AB7	UTP_OP_ADDR[1]		X			X	
AB8	UTP_IP_FCO		X			X	
AB9	UTP_IP_ADDR[1]		X			X	
AB10	BYPASS_CLK		X	X	X	X	X
AB11	HIGHZ_N		X	X	X	X	X
AB12	JTAG_TDO		X	X	X	X	X
AB13	JTG_TCK		X	X	X	X	X
AB14	VCC33		X	X	X	X	X
AB15	EX_ADDR[20]		X	X	X	X	X
AB16	EX_CS_N[1]		X	X	X	X	X
AB17	EX_ADDR[22]		X	X	X	X	X
AB18	EX_ADDR[19]		X	X	X	X	X
AB19	EX_ADDR[18]		X	X	X	X	X
AB20	VSS		X	X	X	X	X
AB21	EX_DATA[9]		X	X	X	X	X
AB22	VSS		X	X	X	X	X
AB23	EX_DATA[6]		X	X	X	X	X
AB24	EX_DATA[3]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 23 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
AC1	VCC33		X	X	X	X	X
AC2	VCC33		X	X	X	X	X
AC3	UTP_OP_DATA[2]	ETHA_TXDATA[2]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AC4	UTP_IP_DATA[4]	ETHA_RXDV	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AC5	UTP_IP_DATA[0]	ETHA_RXDATA[0]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AC6	UTP_OP_ADDR[3]		X			X	
AC7	VCC33		X	X	X	X	X
AC8	UTP_IP_CLK	ETHA_RXCLK	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AC9	RESET_IN_N		X	X	X	X	X
AC10	VSS		X	X	X	X	X
AC11	JTAG_TDI		X	X	X	X	X
AC12	JTAG_TRST_N		X	X	X	X	X
AC13	VSS		X	X	X	X	X
AC14	EX_RD_N		X	X	X	X	X
AC15	EX_WR_N		X	X	X	X	X
AC16	EX_ALE		X	X	X	X	X
AC17	EX_CS_N[3]		X	X	X	X	X
AC18	EX_CS_N[0]		X	X	X	X	X
AC19	EX_ADDR[21]		X	X	X	X	X
AC20	EX_ADDR[14]		X	X	X	X	X
AC21	EX_ADDR[12]		X	X	X	X	X
AC22	EX_CLK		X	X	X	X	X
AC23	EX_DATA[8]		X	X	X	X	X
AC24	EX_DATA[7]		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

Table 26. Processors' Ball Map Assignments (Sheet 24 of 24)

Ball	Signal Name		Processor Number				
	Configuration 1	Configuration 2	Intel® IXP435 Network Processor	Intel® IXP433 Network Processor	Intel® IXP432 Network Processor	Intel® IXP431 Network Processor	Intel® IXP430 Network Processor
AD1	VSS		X	X	X	X	X
AD2	VCC33		X	X	X	X	X
AD3	UTP_OP_DATA[1]	ETHA_TXDATA[1]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AD4	UTP_IP_DATA[3]	ETHA_RXDATA[3]	X	X Config. 2 only	X Config. 2 only	X Config. 1 only	X Config. 2 only
AD5	UTP_OP_SOC		X			X	
AD6	UTP_OP_ADDR[2]		X			X	
AD7	UTP_IP_FCI		X			X	
AD8	UTP_IP_ADDR[3]		X			X	
AD9	POWER_RESET_N		X	X	X	X	X
AD10	PLL_LOCK		X	X	X	X	X
AD11	JTAG_TMS		X	X	X	X	X
AD12	VCC33		X	X	X	X	X
AD13	OSC_IN		X	X	X	X	X
AD14	OSC_OUT		X	X	X	X	X
AD15	VSS		X	X	X	X	X
AD16	EX_IOWAIT_N		X	X	X	X	X
AD17	VCC33		X	X	X	X	X
AD18	EX_CS_N[2]		X	X	X	X	X
AD19	VSS		X	X	X	X	X
AD20	EX_ADDR[15]		X	X	X	X	X
AD21	VCC33		X	X	X	X	X
AD22	EX_DATA[14]		X	X	X	X	X
AD23	EX_DATA[12]		X	X	X	X	X
AD24	VSS		X	X	X	X	X

Notes:

1. Interfaces not being utilized at a system level can require either an external pull-up or pull-down resistors. For detailed information and requirements, refer to Section 4.1, "Functional Signal Definitions" on page 36.
2. Configuration 1 and 2 are set by the Expansion bus configuration when Reset is deasserted. For more information, refer to the UTOPIA/Ethernet Configuration Options table in the Expansion Bus subsection of the *Intel® IXP43X Product Line of Network Processors Developer's Manual*
3. *Blank field* indicates that there is no physical ball on package.

4.4 Package Thermal Specifications

The thermal parameter defined in Table 27 is based on simulated results of packages assembled on standard multi-layer, 2s2p, 1.0-oz copper layer boards in a natural convection environment. The maximum case temperature is based on the maximum junction temperature and defined by the relationship:

T_{case} max = T_{jmax} - (Ψ_{JT} x Power)

Where Ψ_{JT} is the junction-to-package top thermal characterization parameter. If the case temperature exceeds the specified T_{case} max, thermal enhancements such as heat sinks or forced air is required. In the tables below, Θ_{JA} is the package junction-to-air thermal resistance.

Table 27. Package Thermal Characteristics

Package Type	Estimated Power (TPD)	Θ_{JA}	Ψ_{JT}	T_{case} Max. †
31x31mm PBGA	2.7 W	17.3°C/W	1.6 °C/W	106 °C
† This should not exceed the maximum allowable case temperature				

5.0 Electrical Specifications

5.1 Absolute Maximum Ratings and Operating Conditions

Table 28. Absolute Maximum Ratings

Parameter	Maximum Rating
Ambient Air Temperature (Extended)	-40° C to 85° C
Ambient Air Temperature (Commercial)	0° C to 70° C
Storage Temperature	-55°C to 125° C

Table 29. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{CC33}	Voltage supplied to the I/O, with the exception of the DDRII/I SDRAM Interface.	3.135	3.3	3.465	V	
V_{CC}	Voltage supplied to the internal logic. (400, 533, and 667 MHz)	1.235	1.3	1.365	V	
V_{CCDDR}	Voltage supplied to the DDRI SDRAM Interface. Voltage supplied to the DDRII SDRAM Interface.	2.375 1.71	2.5 1.8	2.625 1.89	V V	
V_{CCP_OSC}	Voltage supplied to the oscillator I/O.	3.135	3.3	3.465	V	
USB_V5ref	5V Vref input voltage	4.75	5	5.25	V	1
V_{CCPUSB}	Voltage supplied to the USB I/O.	3.135	3.3	3.465	V	
V_{CCAUBG}	Voltage supplied to the USB Band Gap.	3.135	3.3	3.465	V	
V_{AUPLL}	Voltage supplied to the USB phase-lock loop.	1.235	1.3	1.365	V	
$V_{CCUSBCORE}$	Voltage supplied to the USB I/O core	1.235	1.3	1.365	V	
V_{CCA}	Voltage supplied to the analog phase-lock loop.	1.235	1.3	1.365	V	

Note:
1. When the USB_V5ref pin is tied to 3.3V instead of 5v, the pin cannot withstand short circuit stress to Vbus(5V) and the parts are damaged if there is a short circuit in Vbus.

Warning: Operating beyond the **absolute maximum ratings or operating conditions** is not recommended and functional operation is not guaranteed. Exposure beyond these can affect device reliability and may cause permanent damage.

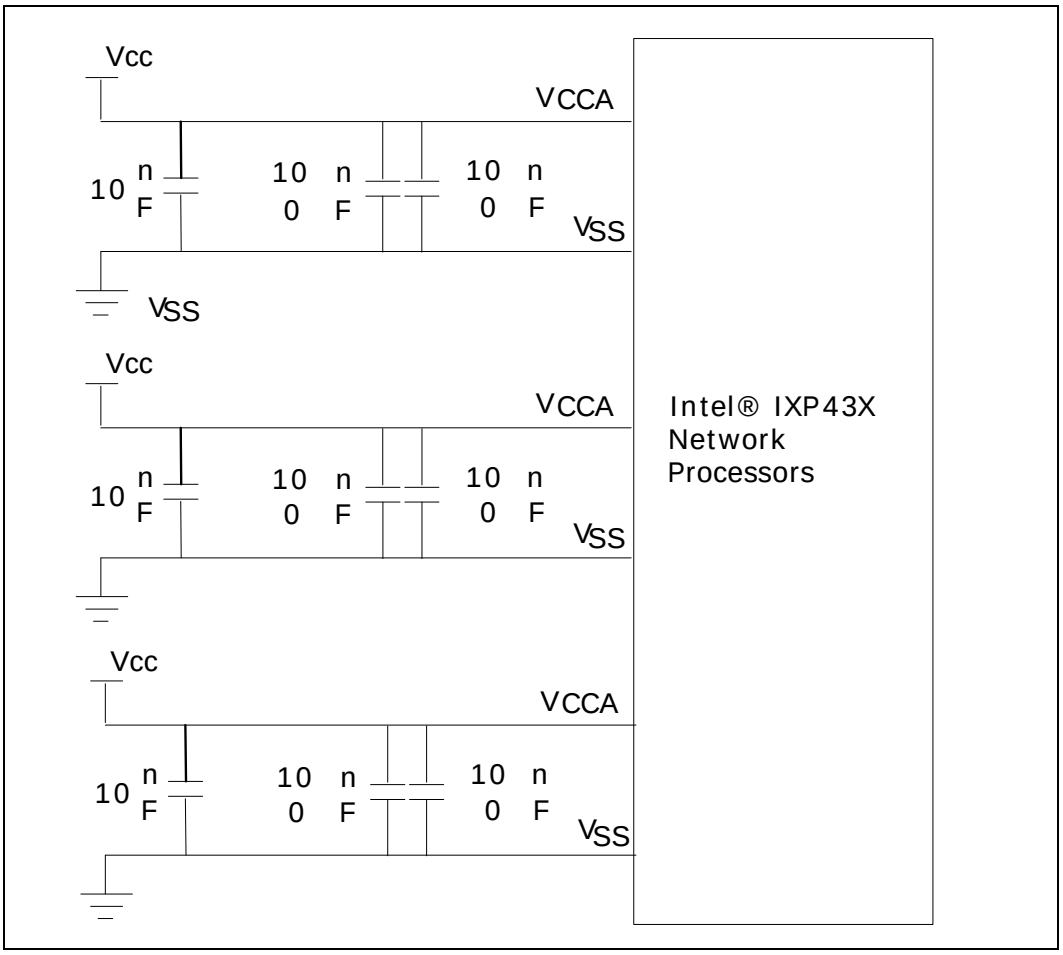
5.2 V_{CCA}, V_{CCP_OSC}, $V_{CCAUPLL}$ and V_{CCAUBG} Pin Requirements

To reduce voltage-supply noise on the analog sections of the IXP43X network processors, the phase-lock loop circuits (V_{CCA}) and oscillator circuit (V_{CCP_OSC}) require isolated voltage supplies. The filter circuits for each supply are shown in the following sections.

5.2.1 V_{CCA} Requirements

1. A parallel combination of a 10-nF capacitor for bypass, and a 200-nF capacitor for first-order filter with a cut-off frequency below 30 MHz should be connected to each of the three V_{CCA} pins of the IXP43X network processors.
2. The ground of both the capacitors should be connected to the nearest V_{SS} supply pin. Both the capacitors should be located less than 0.5 inch away from the V_{CCA} pin and the associated V_{SS} pin. To achieve the 200-nF capacitance, a parallel combination of two 100-nF capacitors can be used as long as the capacitors are placed directly besides each other.

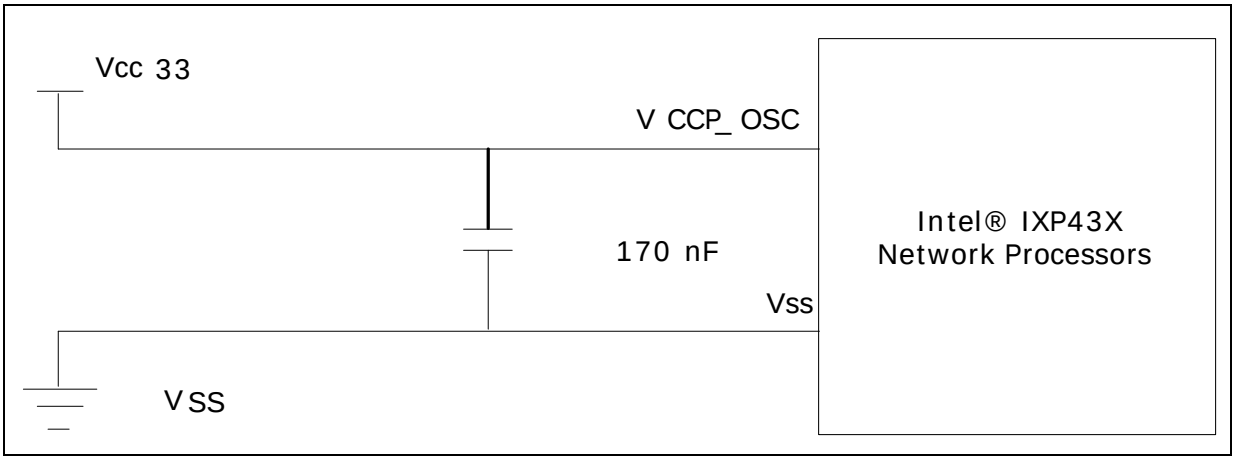
Figure 9. V_{CCA} Power Filtering Diagram



5.2.2 V_{CCP_OSC} Requirements

1. A single, 170-nF capacitor is connected between the V_{CCP_OSC} pin and V_{SS} pin of the IXP43X network processors. This capacitor value provides both bypass and filtering. If the 170 nF is an inconvenient size, capacitor values between 150 nF to 200 nF can be used with little adverse effects, assuming that the effective series resistance of the 200-nF capacitor is under 50 mΩ.
2. To achieve a 200-nF capacitance, a parallel combination of two 100-nF capacitors can be used as long as the capacitors are placed directly besides each other.

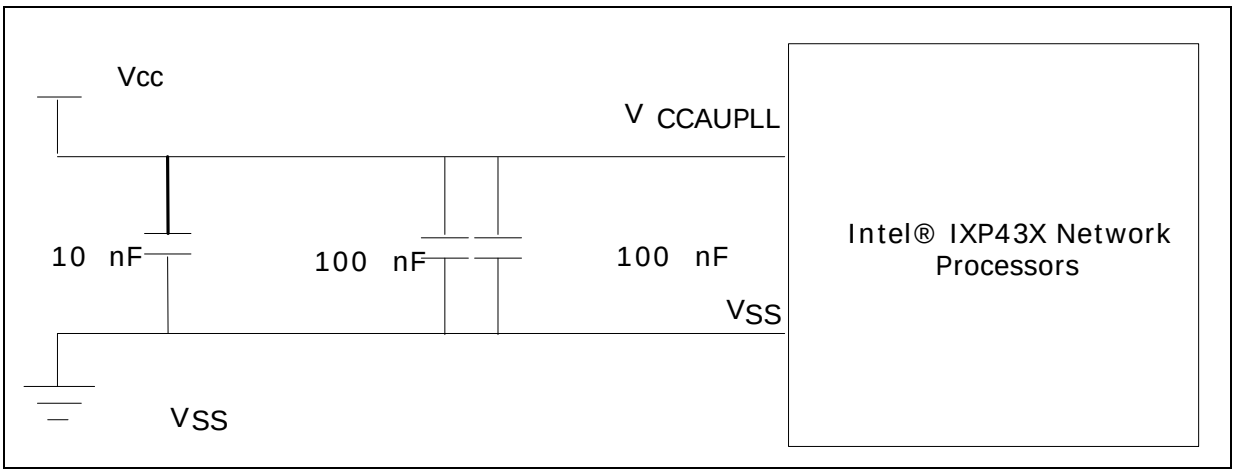
Figure 10. V_{CCP_OSC} Power Filtering Diagram



5.2.3 $V_{CCAUPLL}$ Requirements

1. A parallel combination of a 10-nF capacitor for bypass, and a 200-nF capacitor for first-order filter with a cut-off frequency below 30 MHz should be connected to the $V_{CCAUPLL}$ pin of the IXP43X network processors.
2. The ground of both the capacitors should be connected to the nearest V_{SS} supply pin. Both the capacitors should be located less than 0.5 inch away from the $V_{CCAUPLL}$ pin and the associated V_{SS} pin. To achieve the 200-nF capacitance, a parallel combination of two 100-nF capacitors can be used as long as the capacitors are placed directly besides each other.

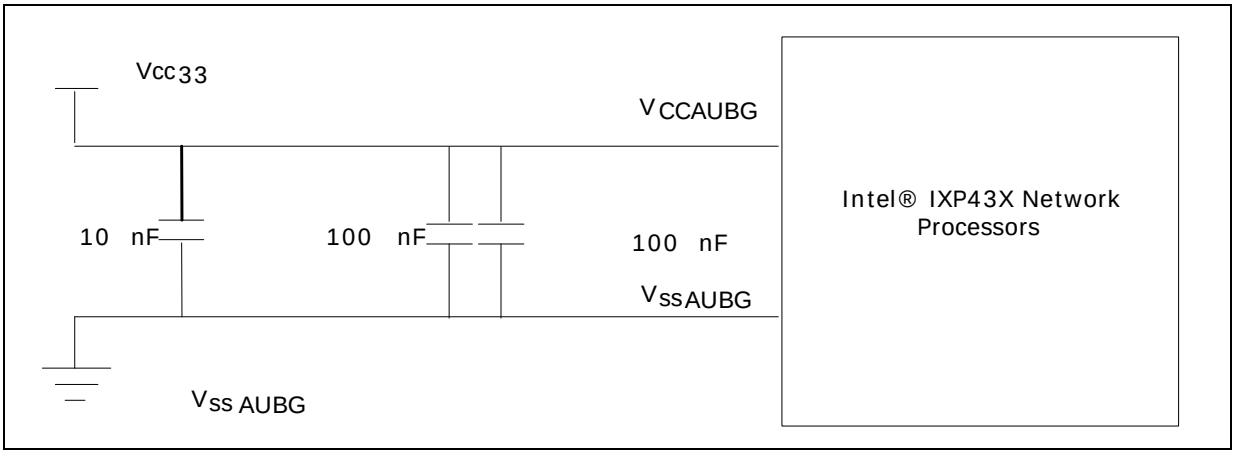
Figure 11. $V_{CCAUPLL}$ Power Filtering Diagram



5.2.4 V_{CCAUBG} Requirements

1. A parallel combination of a 10-nF capacitor for bypass, and a 200-nF capacitor for first-order filter with a cut-off frequency below 30 MHz should be connected to the V_{CCAUBG} pin of the IXP43X network processors.
2. The ground of both the capacitors should be connected to the V_{SSAUBG} pin of the IXP43X network processors, which can be connected to the main V_{SS} plane on the board. Both the capacitors should be located less than 0.5 inch away from the V_{CCAUBG} pin and the associated V_{SSAUBG} pin. To achieve the 200-nF capacitance, a parallel combination of two 100-nF capacitors can be used as long as the capacitors are placed directly besides each other.

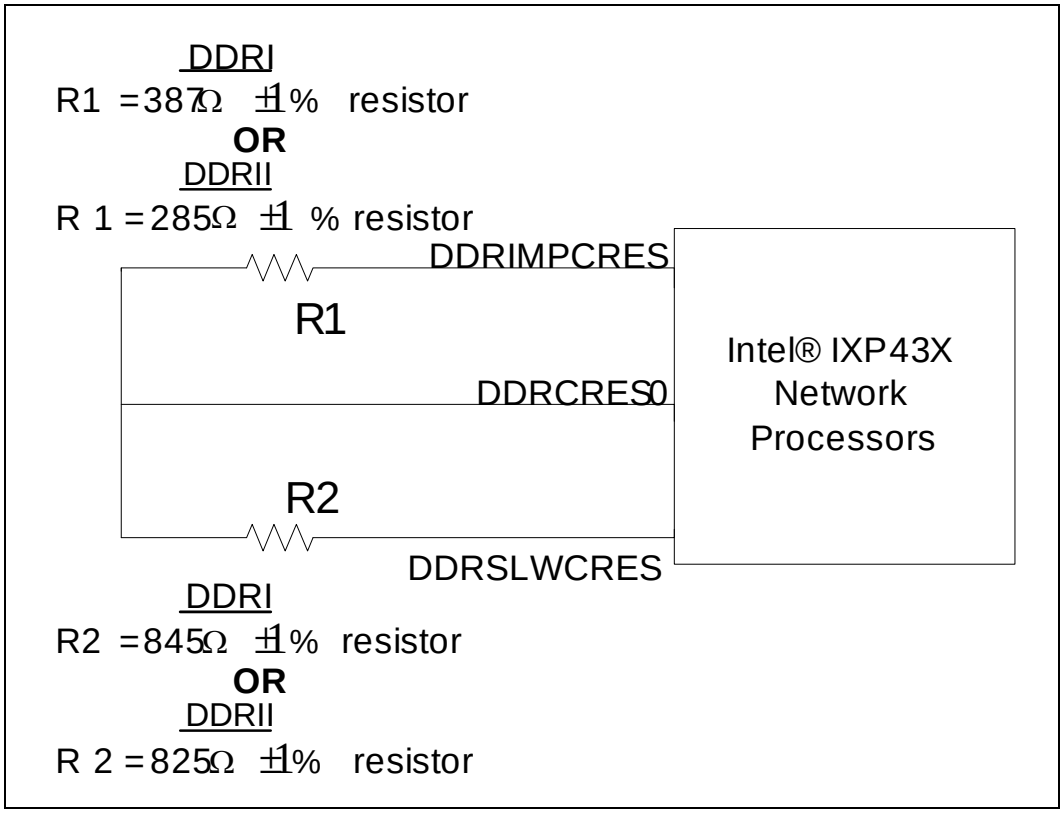
Figure 12. V_{CCAUBG} Power Filtering Diagram



5.3 DDRII/DDRI RCOMP and Slew Resistances Pin Requirements

Figure 13 shows the requirements for DDRII/DDRI RCOMP pin.

Figure 13. DDRII/DDRI RCOMP Pin External Resistor Requirements

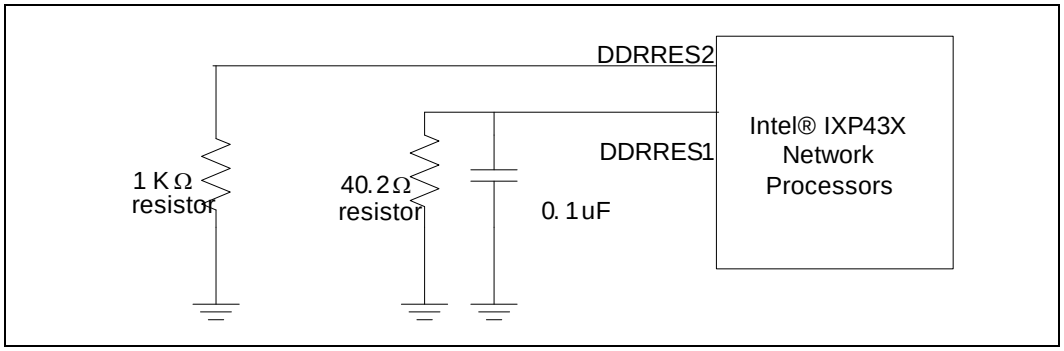


For example, when DDRI SDRAM is used, DDRIMPCRES is connected with 387Ω and DDRSLWCRES is connected with 845Ω resistor to DDRCRES0.

5.4 DDRII OCD Pin Requirements

Figure 14 shows the requirement for DDRRES1 and DDRRES2 pins.

Figure 14. DDRII OCD Pin Requirements

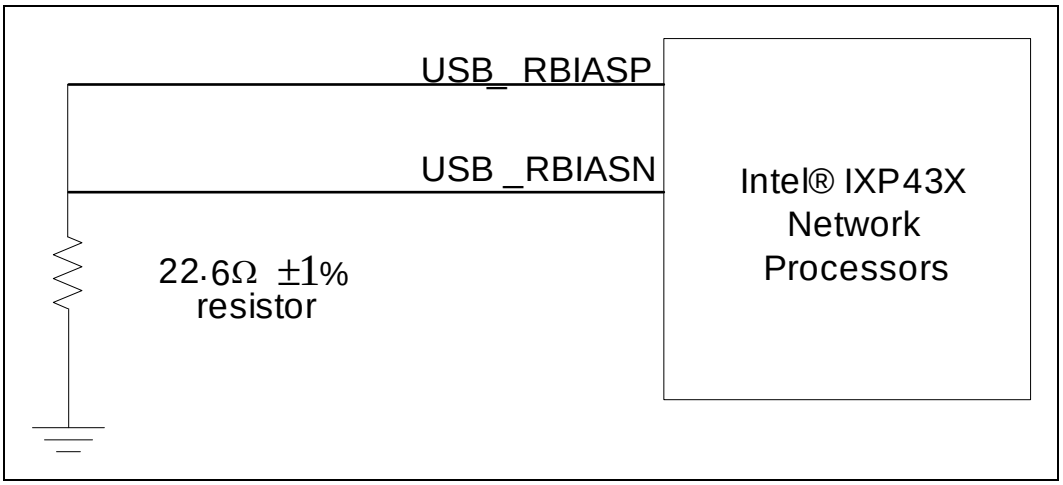


Note: Since the OCD calibration function is not enabled, DDRRES2 must be pulled to ground with a 1-KΩ resistor.

5.5 USB RCOMP and ICOMP Pin Requirements

Figure 15 shows the requirement for USB RCOMP and ICOMP Pins.

Figure 15. USB RCOMP and ICOMP Pin External Resistor Requirement



5.6 DC Specifications

This section contains information regarding the interface DC specifications. Table 30 summarizes the DC specifications sections.

Table 30. DC Specifications Summary

Reference
Table 31, “PCI DC Parameters” on page 92
Table 32, “USB DC Parameters” on page 93
Table 33, “UTOPIA Level 2 DC Parameters” on page 94
Table 34, “MII DC Parameters” on page 94
Table 35, “MDI DC Parameters” on page 94
Table 36, “DDRI SDRAM Bus DC Parameters” on page 95
Table 37, “DDRII DC Parameters” on page 95
Table 38, “Expansion Bus DC Parameters” on page 96
Table 39, “High-Speed Serial Interface DC Parameters” on page 96
Table 40, “UART DC Parameters” on page 97
Table 41, “Serial Peripheral Interface DC Parameters” on page 97
Table 42, “GPIO DC Parameters” on page 97
Table 43, “JTAG DC Parameters” on page 98
Table 44, “PWRON_RESET _N and RESET_IN_N Parameters” on page 98
Table 45, “Remaining I/O DC Parameters (JTAG, PLL_LOCK)” on page 98

5.6.1 PCI DC Parameters

Table 31. PCI DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		0.5 V_{CC33}			V	3
V_{IL}	Input-low voltage				0.3 V_{CC33}	V	3
V_{OH}	Output-high voltage	I_{OUT} = -500 µA	0.9 V_{CC33}			V	3
V_{OL}	Output-low voltage	I_{OUT} = 1500 µA			0.1 V_{CC33}	V	3
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CC33}	-10		10	µA	1, 3
C_{IN}	Input-pin capacitance			5		pF	2, 3
C_{OUT}	I/O or output pin capacitance			5		pF	2,3
C_{IDSEL}	IDSEL-pin capacitance			5		pF	2,3
L_{PIN}	Pin inductance			20		nH	2,3

Note:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state output.
2. These values are typical values seen during manufacturing process and are not tested.
3. For additional information, see the *PCI Local Bus Specification*, Revision 2.2.

5.6.2 USB DC Parameters

Table 32. USB DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
Supply Voltage							
USB_V5ref	5V Vref input voltage		4.75	5	5.25	V	1
V_{CCPUSB}	Voltage supplied to the USB I/O.		3.135	3.3	3.465	V	
$V_{CCUSBCORE}$	Voltage supplied to the USB I/O core.		1.235	1.3	1.365	V	
V_{CCAUBG}	Voltage supplied to the USB band gap.		3.135	3.3	3.465	V	
V_{AUPLL}	Voltage supplied to the USB phase-lock loop.		1.235	1.3	1.365	V	
V_{IL}	Input-low voltage				0.8	V	
V_{DI}	Differential input sensitivity		0.2			V	
V_{CM}	Differential common mode range	Includes V_{DI}	0.8		2.5	V	
V_{OL}	Output-low voltage	IOUT = 6.1 * V_{OH}mA			0.3	V	
V_{OH}	Output-high voltage	I_{OUT} = -6.1 * V_{OH}mA	2.8		3.6	V	
High Speed Receiver							
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV	
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		625	mV	
V_{HSCM}	High-speed data signaling common mode voltage range		-50		500	mV	
V_{HSOL}	High-speed idle level		-10		10	mV	
High Speed Transmitter							
V_{HSOH}	High-speed data signalling high		360		440	mV	
V_{HSOL}	High-speed data signalling low		-10		10	mV	

Note:
1. When the USB_V5ref pin is tied to 3.3V instead of 5v, the pin cannot withstand short circuit stress to Vbus(5V) and the parts are damaged if there is a short circuit in Vbus.

5.6.3 UTOPIA Level 2 DC Parameters

Table 33. UTOPIA Level 2 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = -8 mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 8 mA			0.5	V	
I_{OH}	Output current at high voltage	V_{OH} > 2.4 V	-8			mA	
I_{OL}	Output current at low voltage	V_{OL} < 0.5 V	8			mA	
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CC33}	-10		10	µA	1
C_{IN}	Input-pin capacitance			5		pF	2
C_{OUT}	I/O or output pin capacitance			5		pF	2

Note:
1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state output.
2. These values are typical values seen during manufacturing process and are not tested.

5.6.4 MII DC Parameters

Table 34. MII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = - 6 mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 6 mA			0.4	V	
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CC33}	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.

5.6.5 Management Data Interface (MDI) DC Parameters (MDC, MDIO)

Table 35. MDI DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = - 6 mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 6 mA			0.4	V	
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CC33}	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.

5.6.6 DDR SDRAM Bus DC Parameters

Table 36. DDRI SDRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{DDR_VREF}	I/O Reference voltage		0.49*V_{CCDDR}		0.51*V_{CCDDR}	V	
V_{IH}	Input-high voltage		V_{DDR_VREF} +0.18		V_{CCDDR}+0.3	V	2
V_{IL}	Input-low voltage		-0.3		V_{DDR_VREF} -0.22	V	2
V_{OH}	Output-high voltage	I_{OUT} = -12.5mA	1.95			V	2
V_{OL}	Output-low voltage	I_{OUT} = 12.5mA			0.35	V	2
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CCDDR}	-10		10	µA	
C_{IO}	I/O-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.
2. Only 2.5V DDRI SDRAM is supported while complying to these DC parameters

Table 37. DDRII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{DDR_VREF}	I/O Reference voltage		0.49*V_{CCDDR}		0.51*V_{CCDDR}	V	
V_{IH}	Input-high voltage		V_{DDR_VREF} + 0.125		V_{CCDDR}+0.2	V	2
V_{IL}	Input-low voltage		-0.2		V_{DDR_VREF} - 0.125	V	2
V_{OH}	Output-high voltage	I_{OUT} = -18 mA	1.314			V	2
V_{OL}	Output-low voltage	I_{OUT} = 20.7 mA			0.414	V	2
I_{IL}	Input-leakage current	0 < V_{IN} < V_{CC33}	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.
2. Only 1.8V DDRII SDRAM is supported while complying to these DC parameters

5.6.7 Expansion Bus DC Parameters

Table 38. Expansion Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OHDRV0}	Output-high voltage	I_{OUT} = -8 mA	2.4			V	1, 2
V_{OLDRV0}	Output-low voltage	I_{OUT} = 8 mA			0.4	V	1, 2
V_{OHDRV1}	Output-high voltage	I_{OUT} = -14 mA	2.4			V	1, 3
V_{OLDRV1}	Output-low voltage	I_{OUT} = 14mA			0.4	V	1, 3
V_{OHDRV2}	Output-high voltage	I_{OUT} = -20 mA	2.4			V	1, 4
V_{OLDRV2}	Output-low voltage	I_{OUT} = 20 mA			0.4	V	1, 4
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	2

Note:
1. These values are typical values seen during manufacturing process and are not tested.
2. The values represented with this voltage parameter is used in a system in which the expansion bus interfaces a single load of 6pF placed less than 2 inches away from the IXP43X network processors. This drive strength setting should be used to avoid ringing when minimal loading is attached. Use IBIS models and simulation tools to guarantee the design.
3. The values represented with this voltage parameter is used in a system in which the expansion bus interfaces four loads of 6pF each. All components are placed no further than 4 inches away from the IXP43X network processors. This drive strength setting should be used to avoid ringing when medium loading is attached. Use IBIS models and simulation tools to guarantee the design.
4. The values represented with this voltage parameter is used in a system in which the expansion bus interfaces eight loads of 6pF and all components are placed less than 6 inches from the IXP43X network processors. Another use case of this drive strength is four loads of 6pF operating at 80MHz. This drive strength setting should be used to avoid ringing when maximum loading or frequency is utilized. Use IBIS models and simulation tools to guarantee the design.

5.6.8 High-Speed Serial Interface DC Parameters

Table 39. High-Speed Serial Interface DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = N/A	2.4			V	2
V_{OL}	Output-low voltage	I_{OUT} = 6mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.
2. This is an open drain output; the part exhibits no drive in this operation and the 2.4V is specified to be achieved through an external board pull-up.

5.6.9 UART DC Parameters

Table 40. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = - 4mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 4mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during the manufacturing process and are not tested.
2. This interface is designed assuming a single load that is between 5pF to 25pF.

5.6.10 Serial Peripheral Interface DC parameters

Table 41. Serial Peripheral Interface DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = - 6mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 6mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1.0

Note:
1. These values are typical values seen during manufacturing process and are not tested.

5.6.11 GPIO DC Parameters

Table 42. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage for GPIO 0 to GPIO 13	I_{OUT} = -16 mA	2.4			V	
V_{OL}	Output-low voltage for GPIO 0 to GPIO 13	I_{OUT} = 16 mA			0.4	V	
V_{OH}	Output-high voltage for GPIO 14 and GPIO 15	I_{OUT} = -4 mA	2.4			V	
V_{OL}	Output-low voltage for GPIO 14 and GPIO 15	I_{OUT} = 4 mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Note:
1. These values are typical values seen during manufacturing process and are not tested.

5.6.12 JTAG DC Parameters

Table 43. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = -4 mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 4 mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1

Notes:
1. These values are typical values seen during manufacturing process and are not tested.

5.6.13 Reset DC Parameters

Table 44. PWRON_RESET _N and RESET_IN_N Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	

5.6.14 Remaining I/O DC Parameters

Table 45. Remaining I/O DC Parameters (JTAG, PLL_LOCK)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage		2.0			V	
V_{IL}	Input-low voltage				0.8	V	
V_{OH}	Output-high voltage	I_{OUT} = - 4mA	2.4			V	
V_{OL}	Output-low voltage	I_{OUT} = 4mA			0.4	V	
I_{IL}	Input-leakage current	$0 < V_{IN} < V_{CC33}$	-10		10	µA	
C_{IN}	Input-pin capacitance			5		pF	1.0

Note:
1. These values are typical values seen during manufacturing process and are not tested.
2. These parameters are only applicable to signal other than power and ground signals.

5.7 AC Specifications

5.7.1 Clock Signal Timings

5.7.1.1 Processors' Clock Timings

Table 46. Devices' Clock Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{IH}	Input-high voltage	2.0			V	
V_{IL}	Input-low voltage			0.8	V	
$T_{FREQUENCY}$	Clock frequency for the oscillator in the IXP43X network processors	33.33	33.33	33.33	MHz	1, 3
$\triangle_{FREQUENCY}$	Clock tolerance over -40° C to 85° C.	-50		50	ppm	
C_{IN}	Input - Pin capacitance of the IXP43X network processors		5		pF	
T_{DC}	Duty cycle	35	50	65	%	2

Note:
1. This value is an oscillator input. Use this value as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.
2. This parameter applies when driving the clock input with an oscillator.
3. Where the IXP43X network processors are configured with an input reference-clock, the slew rate should never be faster than 2.5 V/nS to ensure proper PLL operation. To guarantee PLL operation at the slower slew rate, the Vih and Vil levels must be met at 33.33 MHz frequency.

Table 47. Processors' Clock Timings Spread Spectrum Parameters

Spread-Spectrum Conditions	Min	Max	Notes
Frequency deviation from 33.33 MHz as a percentage	-2.0%	+0.0%	Characterized and guaranteed by design, but not tested. Do not over-clock the PLL input. The A.C. timings is not guaranteed if the device exceeds 33.33 MHz.
Modulation Frequency		50 KHz	Characterized and guaranteed by design, but not tested

Note:
1. When using spread spectrum clocking, other clocks in the system changes frequency over a specified range. This change in other clocks can present some system level limitations. Refer to the application note titled *Spread Spectrum Clocking to Reduce EMI Application Note* while designing a product that utilizes spread spectrum clocking.
2. When using spread spectrum clocking, an external clock to GPIO Pin 1 should be used as the source for the USB 2.0 Host clock. See the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for detailed information.

Figure 16. Typical Connection to an Oscillator

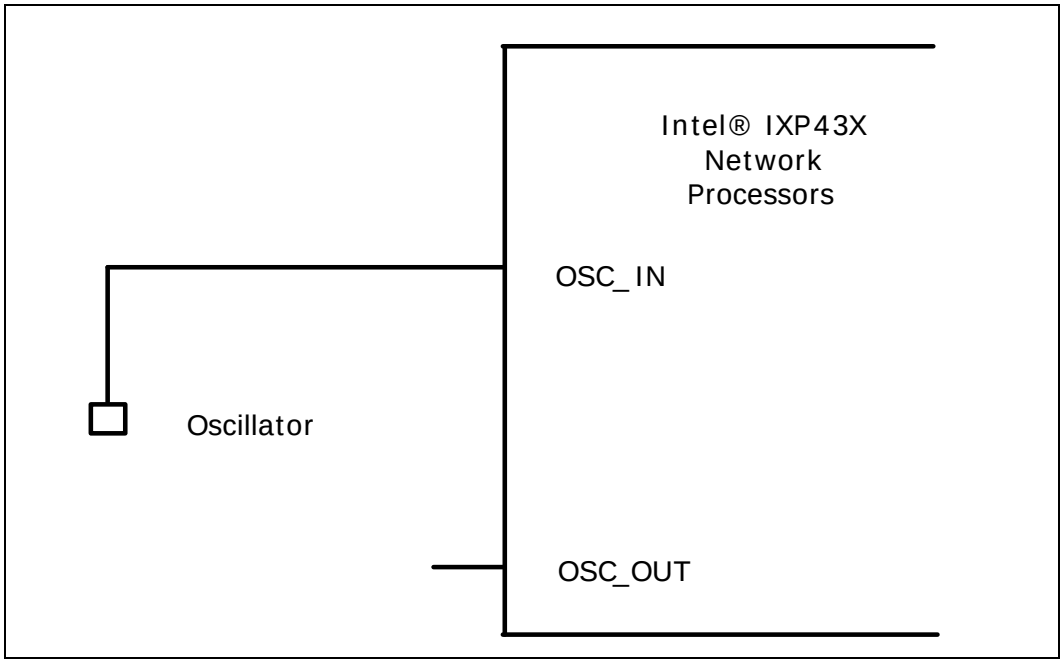
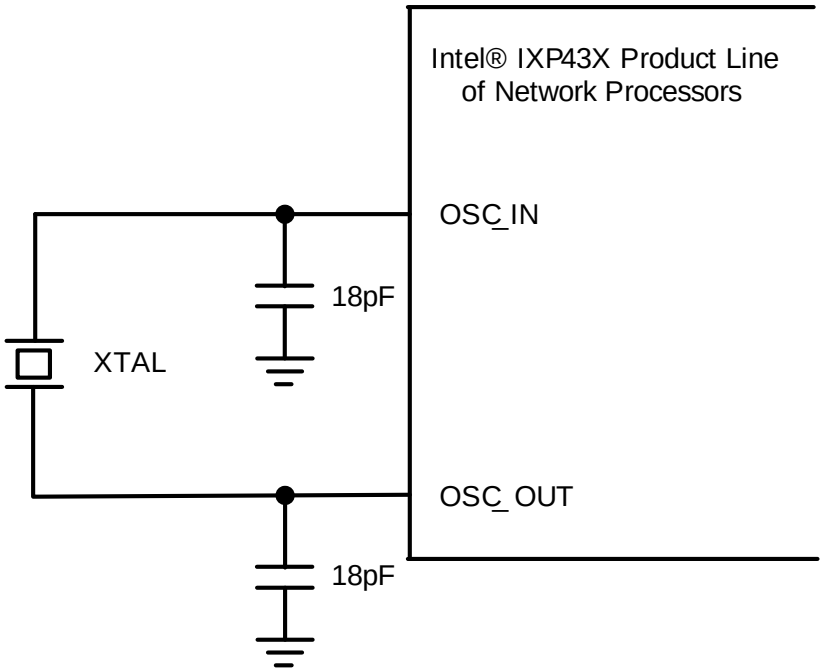


Figure 17. Typical Connection to a Crystal



5.7.1.2 PCI Clock Timings

Table 48. PCI Clock Timings

Symbol	Parameter	33 MHz		Units	Notes
		Min.	Max.		
$T_{PERIODPCICLK}$	Clock period for PCI Clock	30		ns	
$T_{CLKHIGH}$	PCI Clock high time	11		ns	
T_{CLKLOW}	PCI Clock low time	11		ns	
$T_{RISE/FALL}$	Rise and fall time requirements for PCI Clock		2	V/ns	

5.7.1.3 MII Clock Timings

Table 49. MII Clock Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
$T_{period100Mbit}$	Clock period for Tx and Rx Ethernet clocks	40	40		ns	
$T_{period10Mbit}$	Clock period for Tx and Rx Ethernet clocks	400	400		ns	
T_{duty}	Duty cycle for Tx and Rx Ethernet clocks	35	50	65	%	
Frequency Tolerance	Frequency tolerance requirements for Tx and Rx Ethernet clocks		+/- 50	+/- 100	ppm	

5.7.1.4 UTOPIA Level 2 Clock Timings

Table 50. UTOPIA Level 2 Clock Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
T_{period}	Clock period for Tx and Rx UTOPIA Level 2 clocks			30.303	ns	
T_{duty}	Duty cycle for Tx and Rx UTOPIA Level 2 clocks	40	50	60	%	
$T_{rise/fall}$	Rise and fall time requirements for Tx and Rx UTOPIA Level 2 clocks			2	V/ns	

5.7.1.5 Expansion Bus Clock Timings

Table 51. Expansion Bus Clock Timings

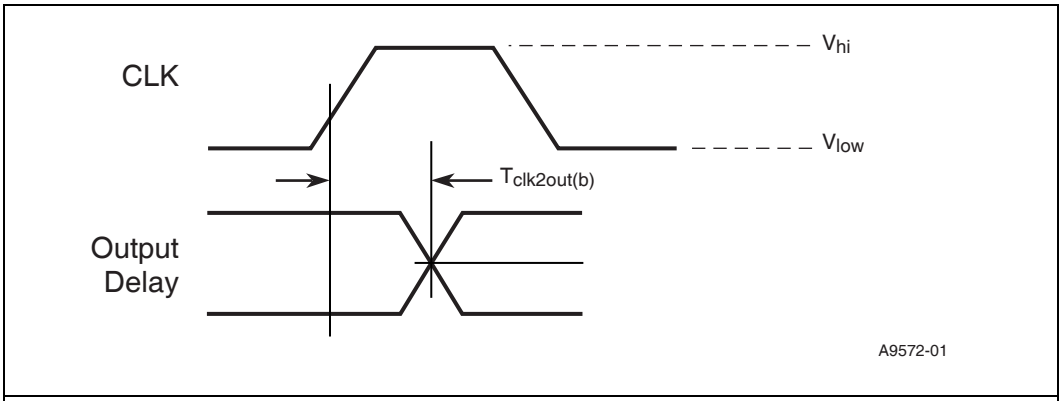
Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
T_{period}	Clock period for expansion-bus clock	12.5			ns	
T_{duty}	Duty cycle for expansion-bus clock	40	50	60	%	
$T_{rise/fall}$	Rise and fall time requirements for expansion-bus clock			2	V/ns	

5.7.2 Bus Signal Timings

The AC timing waveforms are shown in the following sections:

5.7.2.1 PCI

Figure 18. PCI Output Timing



Note: V_{HI} = 0.6 V_{CC} and V_{LOW} = 0.2 V_{CC}.

Figure 19. PCI Input Timing

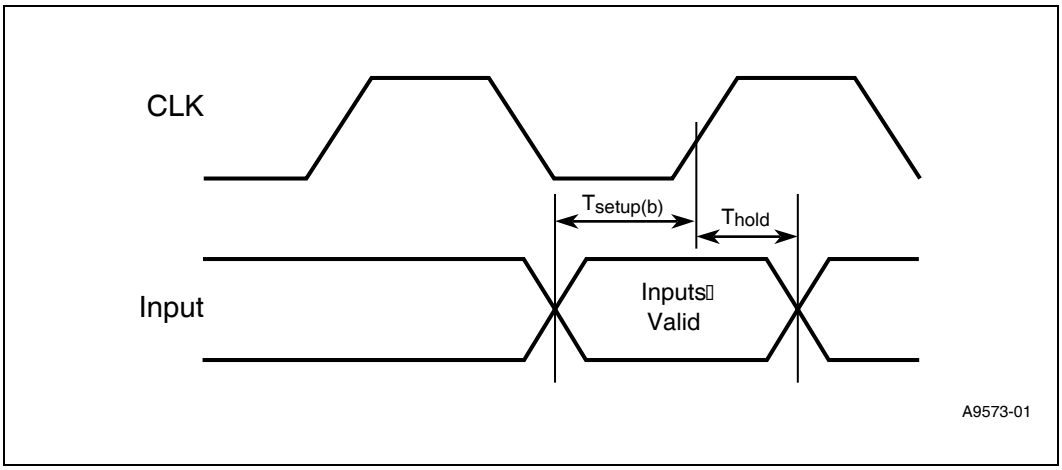


Table 52. PCI Bus Signal Timings

Symbol	Parameter	33 MHz		Units	Notes
		Min.	Max.		
$T_{clk2outb}$	Clock to output for all bused signals. This is the PCI_AD[31:0], PCI_CBE_N [3:0], PCI_PAR, PCI_FRAME_N, PCI_IRDY_N, PCI_TRDY_N, PCI_STOP_N, PCI_DEVSEL_N, PCI_PERR_N, PCI_SERR_N	2	11	ns	1, 2, 5, 7, 8
$T_{clk2out}$	Clock to output for all point-to-point signals. This is the PCI_GNT_N and PCI_REQ_N(0) only.	2	12	ns	1, 2, 5, 7, 8
T_{setupb}	Input setup time for all bused signals. This is the PCI_AD[31:0], PCI_CBE_N [3:0], PCI_PAR, PCI_FRAME_N, PCI_IRDY_N, PCI_TRDY_N, PCI_STOP_N, PCI_DEVSEL_N, PCI_PERR_N, PCI_SERR_N	7		ns	4, 6, 7, 8
T_{setup}	Input setup time for all point-to-point signals. This is the PCI_REQ_N and PCI_GNT_N(0) only.	10, 12		ns	3, 4, 7, 8
T_{hold}	Input hold time from clock.	0		ns	4, 7, 8
$T_{rst-off}$	Reset active-to-output float delay		40	ns	5, 6, 7, 8

Note:
1. See the timing measurement conditions.
2. Parts that are compliant to the 3.3 V signaling environment.
3. REQ_N and GNT_N are point-to-point signals and have different output valid delay and input setup times than do bused signals. GNT_N has a setup of 10 ns for 33 MHz; REQ_N has a setup of 12 ns for 33 MHz.
4. RST_N is asserted and de-asserted asynchronously with respect to CLK.
5. All PCI output to be asynchronously driven to a tri-state value when RST_N is active.
6. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
7. Timing was tested with a 70-pF capacitor to ground.
8. For additional information, refer the *PCI Local Bus Specification*, Revision 2.2.

5.7.2.2 USB Version 2.0 Interface

For timing parameters, see the *USB version 2. 0 specification*. The USB v 2.0 interfaces of the IXP43X network processors support a host only controller.

5.7.2.3 UTOPIA Level 2 (33 MHz)

Figure 20. UTOPIA Level 2 Input Timings

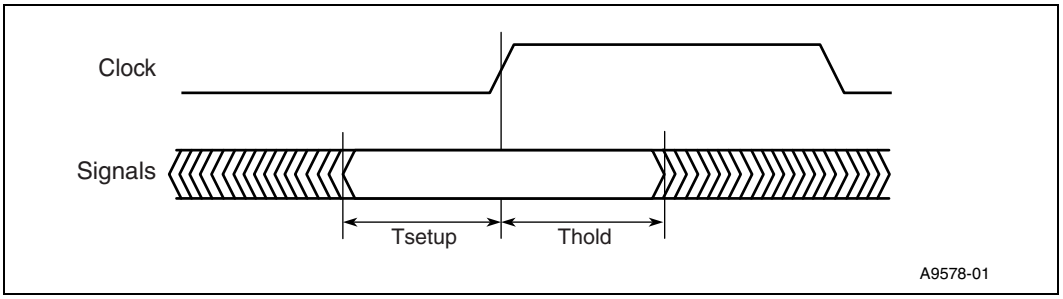


Table 53. UTOPIA Level 2 Input Timings Values

Symbol	Parameter	Min.	Max.	Units	Notes
T_{setup}	Input setup prior to rising edge of clock. Inputs included in this timing are UTP_IP_DATA[7:0], UTP_IP_SOC, AND UTP_IP_FCI, and UTP_OP_FCI.	6		ns	
T_{hold}	Input hold time after the rising edge of the clock. Inputs included in this timing are UTP_IP_DATA[7:0], UTP_IP_SOC, and UTP_IP_FCI, and UTP_OP_FCI.	0		ns	

Figure 21. UTOPIA Level 2 Output Timings

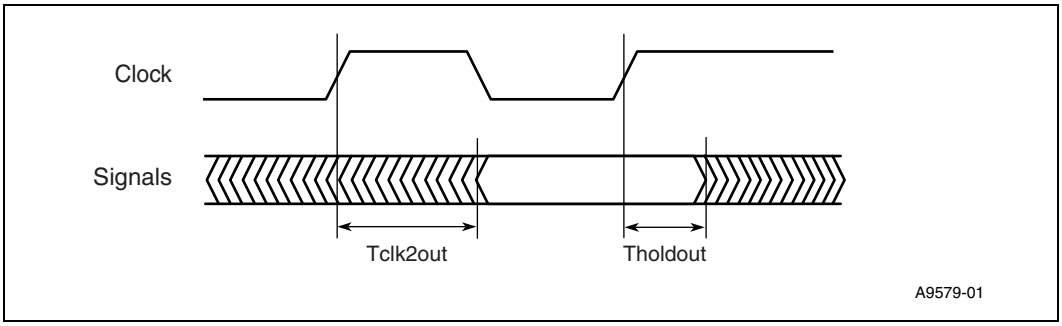


Table 54. UTOPIA Level 2 Output Timings Values

Symbol	Parameter	Min.	Max.	Units	Notes
$T_{clk2out}$	Rising edge of clock to signal output. Output included in this timing are UTP_OP_SOC, UTP_OP_FCO, UTP_IP_FCO, UTP_OP_DATA[7:0], UTP_IP_ADDR[4:0] and UTP_OP_ADDR[4:0].		15	ns	1
$T_{holdout}$	Signal output hold time after the rising edge of the clock. Output included in this timing are UTP_OP_SOC, UTP_OP_FCO, UTP_IP_FCO, UTP_OP_DATA[7:0], UTP_IP_ADDR[4:0] and UTP_OP_ADDR[4:0].	1		ns	1

Note:
1. Timing was designed for system load between 5pF and 25pF

5.7.2.4 MII

Figure 22. MII Output Timings

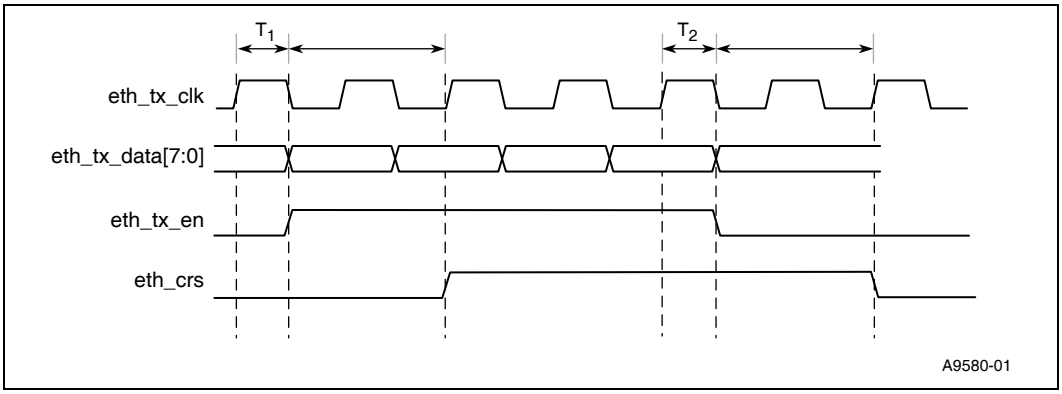


Table 55. MII Output Timings Values

Symbol	Parameter	Min.	Max.	Units	Notes
T_1	Clock to output delay for ETH_TXDATA and ETH_TXEN.		12.5	ns	1, 2
T_2	ETH_TXDATA and ETH_TXEN hold time after ETH_TXCLK.	1.5		ns	2

Note:
1. These values satisfy t the MII specification requirement of 0 ns to 25 ns clock to output delay.
2. Timing was designed for system load between 5 pF and 15 pF.

Figure 23. MII Input Timings

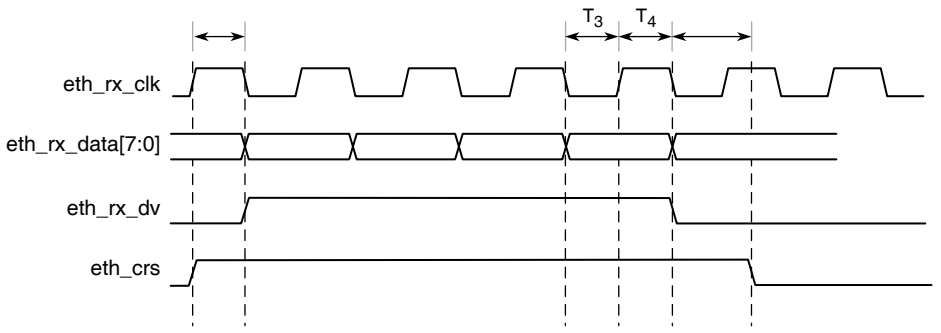


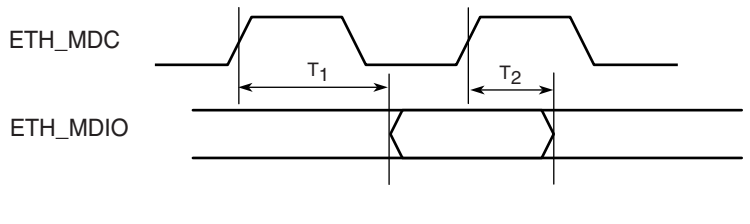
Table 56. MII Input Timings Values

Symbol	Parameter	Min.	Max.	Units	Notes
T_3	ETH_RXDATA and ETH_RXDV setup time prior to rising edge of ETH_RXCLK	5.5		ns	1
T_4	ETH_RXDATA and ETH_RXDV hold time after the rising edge of ETH_RXCLK	0		ns	1, 2

Note:
1. These values satisfy the 10-ns setup and hold time requirements that are necessary for the MII specification.
2. The T4 input hold timing parameter is not 100% tested and is guaranteed by design.

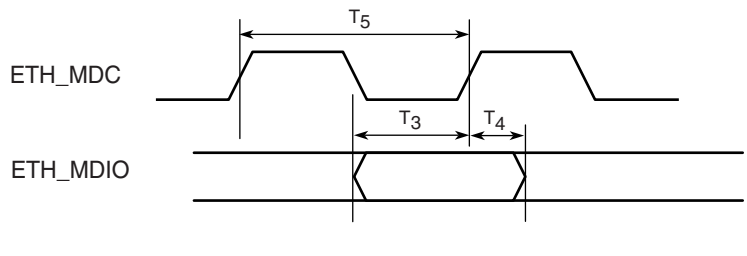
5.7.2.5 MDIO

Figure 24. MDIO Output Timings



Note: Processor is sourcing MDIO.

Figure 25. MDIO Input Timings



Note: PHY is sourcing MDIO.

Table 57. MDIO Timings Values

Symbol	Parameter	Min.	Max.	Units	Notes
T1	ETH_MDIO, clock to output timing with respect to rising edge of ETH_MDC clock		ETH_MDC/2 + 15 ns	ns	
T2	ETH_MDIO output hold timing after the rising edge of ETH_MDC clock	10		ns	
T3	ETH_MDIO input setup prior to rising edge of ETH_MDC clock	3		ns	
T4	ETH_MDIO hold time after the rising edge of ETH_MDC clock	1		ns	
T5	ETH_MDC clock period	125	500	ns	1

Note:
1. Timing was designed for system load between 5pF and 20pF.

5.7.2.6 DDR SDRAM Bus

5.7.2.6.1 DDRI SDRAM Bus

Figure 26. DDR Clock Timing Waveform

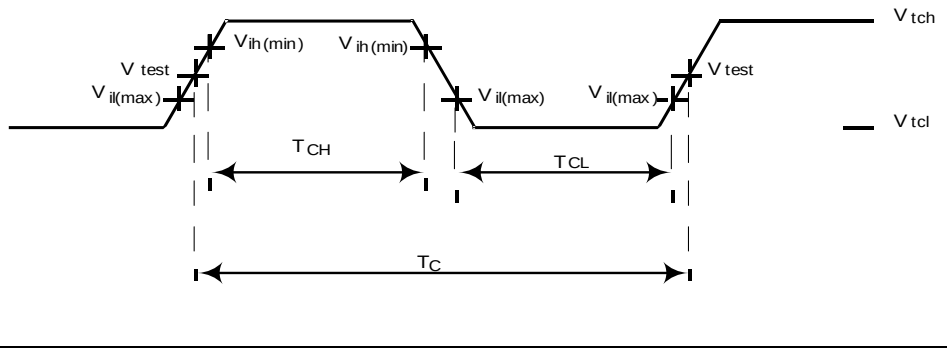


Table 58. DDR Clock Timings

Symbol	Parameter	DDR-II 400		DDR-I 266		Units	Notes
		Min	Max	Min	Max		
T_F	DDR SDRAM clock Frequency		200		133	MHz	
T_C	DDR SDRAM clock Cycle Time	5		7.5		ns	1
T_{CH}	DDR SDRAM clock High Time	2.15		3.37		ns	1
T_{CL}	DDR SDRAM clock Low Time	2.15		3.37		ns	1
T_{CS}	DDR SDRAM clock Period Stability		350		350	ps	
T_{skew}	DDR SDRAM clock skew for any differential clock pair (D_CK[2:0] - D_CK_N[2:0])		100		100	ps	

Notes:
1. See Figure 26, "DDR Clock Timing Waveform" on page 106
2. Vtest is nominally (0.5 * Vtch - Vtcl)

Figure 27. DDR SDRAM Write Timings

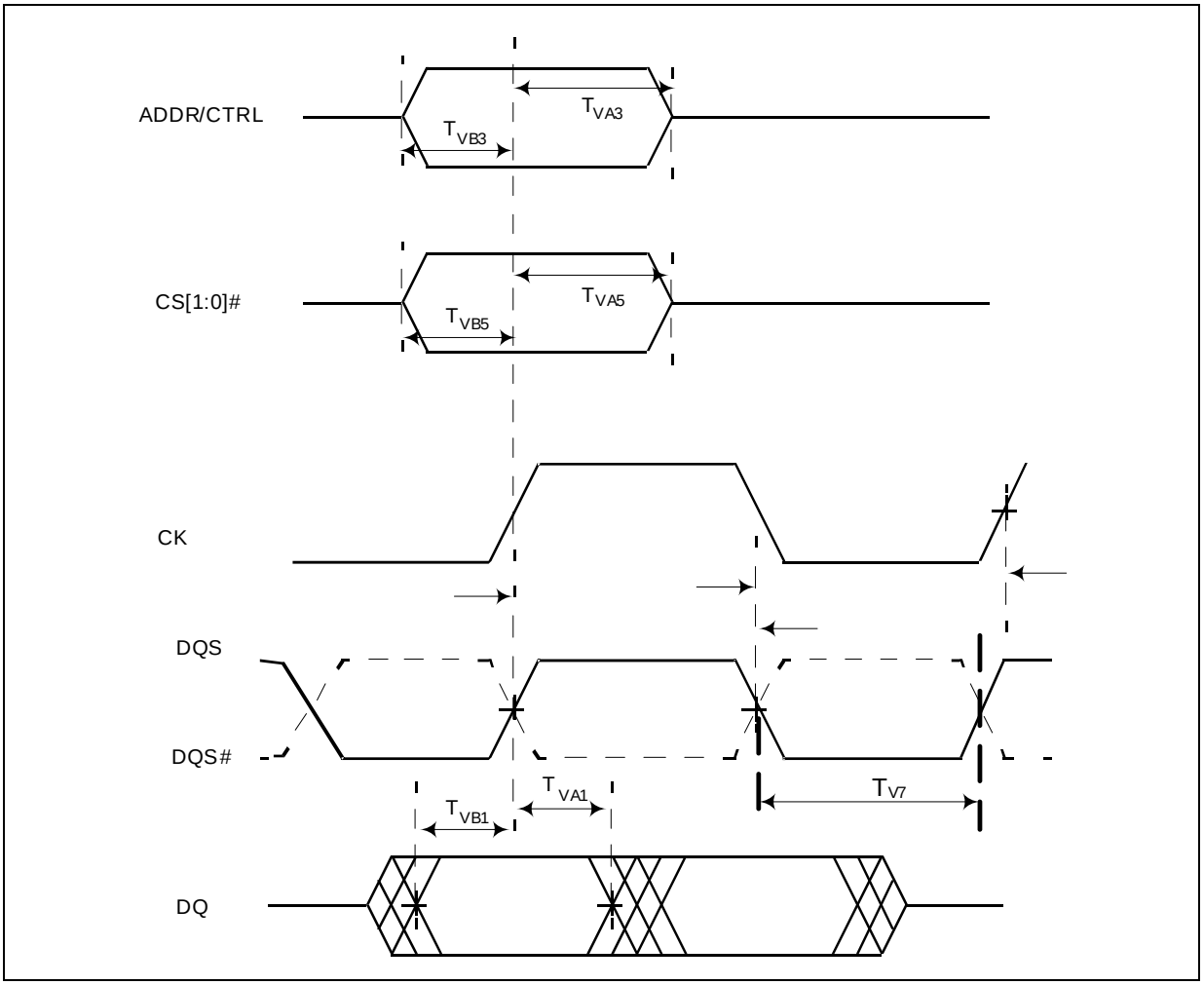


Figure 28. DDR SDRAM Read Timings

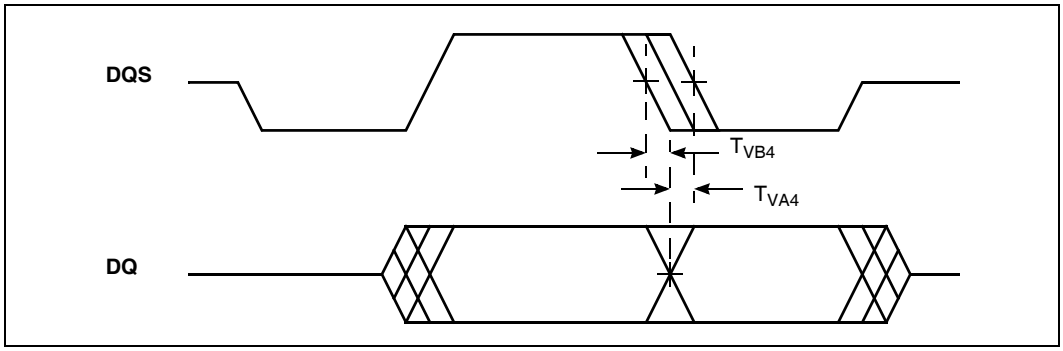


Figure 29. DDR - Write Preamble/Postamble Durations

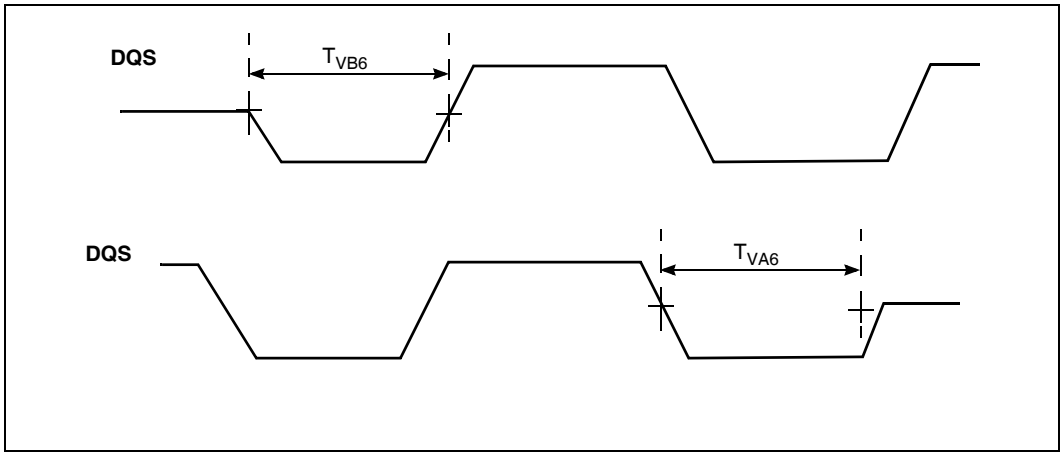


Table 59. DDRII-400 MHz Interface -- Signal Timings

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	521			ps	1
T_{VA1}	DQ, CB and DM write output valid time after DQS.	521			ps	1
T_{VB3}	Address and Command write output valid before CK rising edge.	1771			ps	1, 4
T_{VA3}	Address and Command write output valid after CK rising edge.	1771			ps	1, 4
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	413			ps	2
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	413			ps	2
T_{VB5}	CS_N[1:0] control valid before CK rising edge.	1771			ps	4
T_{VA5}	CS_N[1:0] control valid after CK rising edge.	1771			ps	4
T_{VB6}	DQS write preamble duration.		3750		ps	3
T_{VA6}	DQS write postamble duration.		2500		ps	3
T_{V7}	DQ, CB, and DM pulse width (tDIPW)		1750		ps	1

Notes:
1. See Figure 27, “DDR SDRAM Write Timings” on page 107
2. See Figure 28, “DDR SDRAM Read Timings” on page 108. Data to strobe read setup and data from strobe read hold minimum requirements specified are determined with the DQS delay programmed for 90 degree phase shift.
3. See Figure 29, “DDR - Write Preamble/Postamble Durations” on page 108
4. Address/Command pin group; RAS_N, CAS_N, WE_N, MA[13:0], BA[1:0]
5. Designed to JEDEC specification; it is recommended that IBIS models should be used to verify signal integrity on individual designs

Table 60. DDRI-266 MHz Interface -- Signal Timings

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
T_{VB1}	DQ, CB and DM write output valid time before DQS.	1146			ps	1
T_{VA1}	DQ, CB and DM write output valid time after DQS.	1146			ps	1
T_{VB3}	Address and Command write output valid before CK rising edge.	3021			ps	1, 4
T_{VA3}	Address and Command write output valid after CK rising edge.	3021			ps	1, 4
T_{VB4}	DQ, CB and DM read input valid time before DQS rising or falling edges.	1057			ps	2
T_{VA4}	DQ, CB and DM read input valid time after DQS rising or falling edges.	1057			ps	2
T_{VB5}	CS_N[1:0] control valid before CK rising edge.	3021			ps	4
T_{VA5}	CS_N[1:0] control valid after CK rising edge.	3021			ps	4
T_{VB6}	DQS write preamble duration.		5625		ps	3
T_{VA6}	DQS write postamble duration.		3750		ps	3
T_{V7}	DQ, CB, and DM pulse width (tDIPW)		1750		ps	1

Notes:
1. See Figure 27, “DDR SDRAM Write Timings” on page 107
2. See Figure 28, “DDR SDRAM Read Timings” on page 108. Data to strobe read setup and data from strobe read hold minimum requirements specified are determined with the DQS delay programmed for 90 degree phase shift.
3. See Figure 29, “DDR - Write Preamble/Postamble Durations” on page 108
4. Address/Command pin group; RAS_N, CAS_N, WE_N, MA[13:0], BA[1:0]
5. Designed to JEDEC specification; it is recommended that IBIS models should be used to verify signal integrity on individual designs

5.7.2.7 Expansion Bus

5.7.2.7.1 Expansion Bus Synchronous Operation

Figure 30. Expansion Bus Synchronous Timing

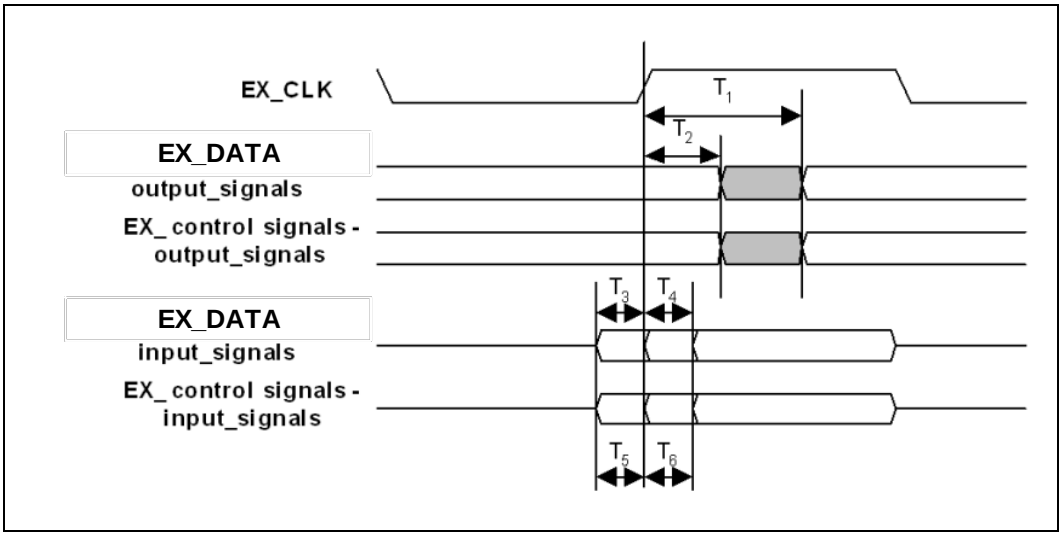


Table 61. Expansion Bus Synchronous Operation Timing Values

Symbol	Parameter	Low Drive		Med Drive		Hi Drive		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_1	Valid rising edge of EX_CLK to valid signal on the output.		10		8.5		6.5	ns	1, 2, 3, 4
T_2	Valid signal hold time after the rising edge of EX_CLK	1		1		1		ns	1, 2, 3, 4
T_3	Valid data signal on an input prior to the rising edge of EX_CLK	2.5		2.5		2.5		ns	1, 2, 3, 4
T_4	Required hold time of a data input after the rising edge of EX_CLK	0.5		0.5		0.5		ns	1, 2, 3, 4
T_5	Valid control/arbiter signal on an input prior to the rising edge of EX_CLK	3.5		3.5		3.5		ns	1, 2, 3, 4
T_6	Required hold time of a control/arbiter input after the rising edge of EX_CLK	0.5		0.5		0.5		ns	1, 2, 3, 4

Notes:
1. Timing was designed for system load between 5pF and 60pF for low drive setting at typically not more than 33 MHz clock
2. Timing was designed for system load between 5pF and 40pF for medium drive setting at typically not more than a 66 MHz clock
3. Timing was designed for system load between 5pF and 25pF for high drive setting at typically not more than a 80 MHz clock
4. Drive settings do not apply to EX_CS_N signals and are expected to be point to point.
5. EX_control_signals output signals comprises the following: EX_ALE, EX_ADDR, EX_CS_N, EX_RD_N, EX_WR_N.

5.7.2.7.2 Expansion Bus Asynchronous Operation

Figure 31. Intel Multiplexed Mode

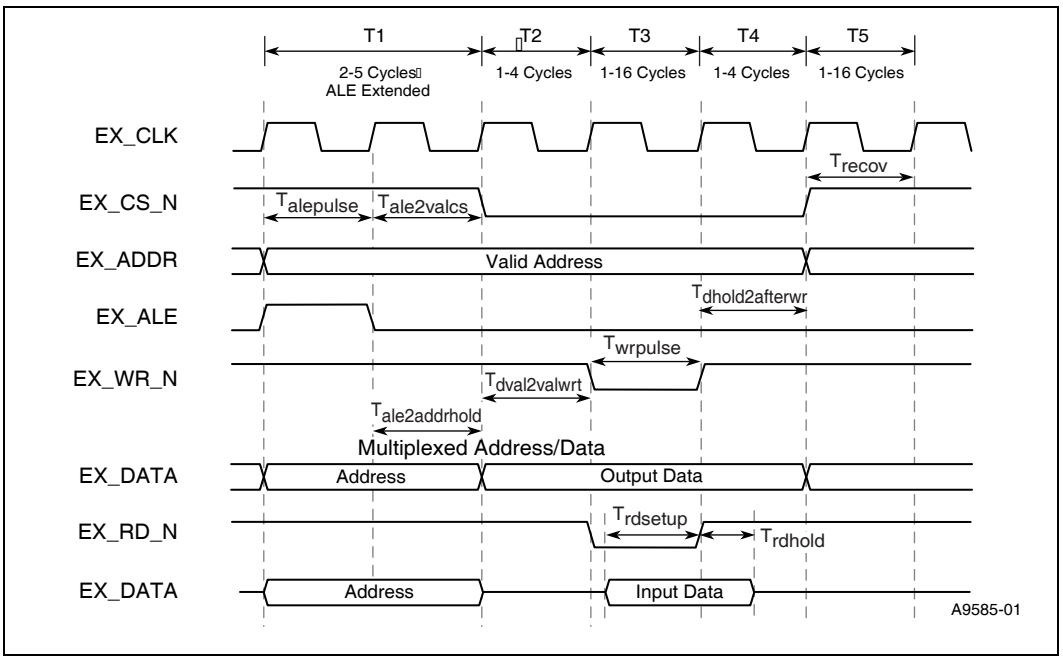


Table 62. Intel Multiplexed Mode Values (Sheet 1 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes
Talepulse	Pulse width of ALE (ADDR is valid at the rising edge of ALE)	1	4	Cycles	1, 7
Tale2addrhold	Valid address hold time after from falling edge of ALE	1	1	Cycles	1, 2, 7
Tdval2valwrt	Write data valid prior to WR_N falling edge	1	4	Cycles	3, 7
Twrpulse	Pulse width of the WR_N	1	16	Cycles	4, 7
Tdholdafterwr	Valid data after the rising edge of WR_N	1	4	Cycles	5, 7
Tale2valcs	Valid chip select after the falling edge of ALE	1	4	Cycles	7

Note:

1. The EX_ALE signal is extended from T to 4Tnsec based on programming of the T1 timing parameter. The parameter Tale2addrhold is fixed at T.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration for which the chip selects, address, and data (during a write) are held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Table 62. Intel Multiplexed Mode Values (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes
Trdsetup	Data valid required before the rising edge of RD_N	14.7		ns	
Trdhold	Data hold required after the rising edge of RD_N	2		ns	
Trecov	Time needed between successive accesses on expansion interface.	1	16	Cycles	6

Note:

1. The EX_ALE signal is extended from T to 4Tnsec based on programming of the T1 timing parameter. The parameter Tale2addrhold is fixed at T.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration for which the chip selects, address, and data (during a write) are held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Figure 32. Intel Simplex Mode

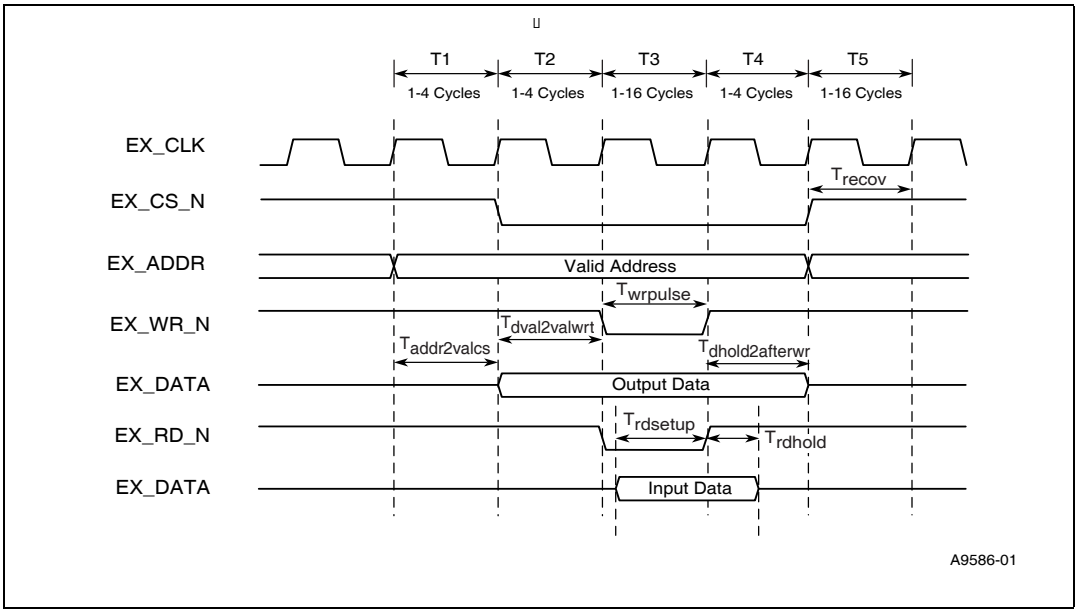


Table 63. Intel Simplex Mode Values

Symbol	Parameter	Min.	Max.	Units	Notes
$T_{addr2valcs}$	Valid address to valid chip select	1	4	Cycles	1, 2, 7
$T_{dval2valwrt}$	Write data valid prior to EXPB_IO_WRITE_N falling edge	1	4	Cycles	3, 7
$T_{wrpulse}$	Pulse width of the EXP_IO_WRITE_N	1	16	Cycles	4, 7
$T_{dholdafterwr}$	Valid data after the rising edge of EXPB_IO_WRITE_N	1	4	Cycles	5, 7
$T_{rdsetup}$	Data valid required before the rising edge of EXP_IO_READ_N	14.7		ns	
T_{rdhold}	Data hold required after the rising edge of EXP_IO_READ_N	2		ns	
T_{recov}	Time required between successive accesses on the expansion interface.	1	16	Cycles	6

Note:
1. EX_ALE is not valid in simplex mode of operation.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration that the chip selects, address, and data (during a write) is held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Figure 33. Motorola* Multiplexed Mode

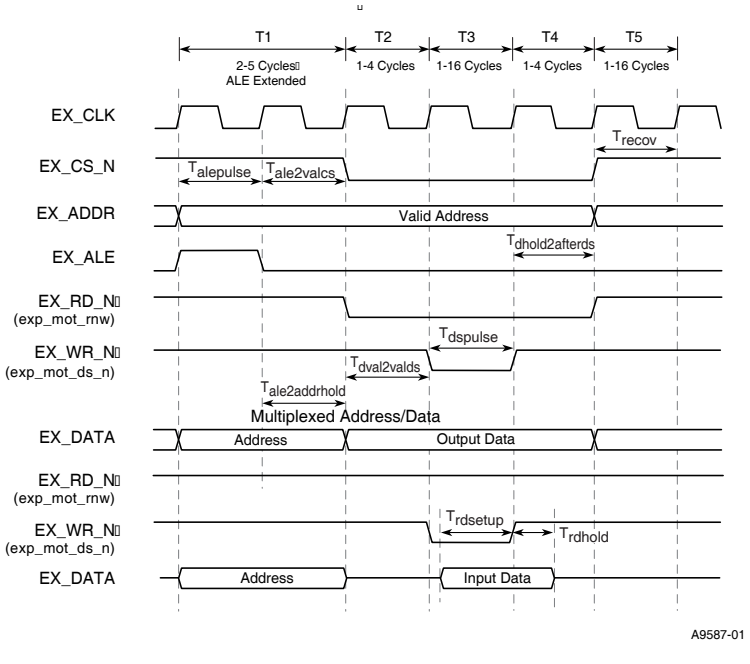


Table 64. Motorola* Multiplexed Mode Values

Symbol	Parameter	Min.	Max.	Units	Notes
$T_{alepulse}$	Pulse width of ALE (ADDR is valid at the rising edge of ALE)	1	4	Cycles	1, 7
$T_{ale2addrhold}$	Valid address hold time after from falling edge of ALE	1	1	Cycles	1, 2, 7
$T_{dval2valds}$	Write data valid prior to EXP_MOT_DS_N falling edge	1	4	Cycles	3, 7
$T_{dspulse}$	Pulse width of the EXP_MOT_DS_N	1	16	Cycles	4, 7
$T_{dholdafterds}$	Valid data after the rising edge of EXP_MOT_DS_N	1	4	Cycles	5, 7
$T_{ale2valcs}$	Valid chip select after the falling edge of ALE	1	4	Cycles	7
$T_{rdsetup}$	Data valid required before the rising edge of EXP_MOT_DS_N	14.7		ns	
T_{rdhold}	Data hold required after the rising edge of EXP_MOT_DS_N	2		ns	
T_{recov}	Time needed between successive accesses on expansion interface.	1	16	Cycles	6

Note:

1. The EX_ALE signal is extended from T to 4Tnsec, based on the programming of the T1 timing parameter. The parameter Tale2addrhold is fixed at T.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration that the chip selects, address, and data (during a write) is held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Figure 34. Motorola* Simplex Mode

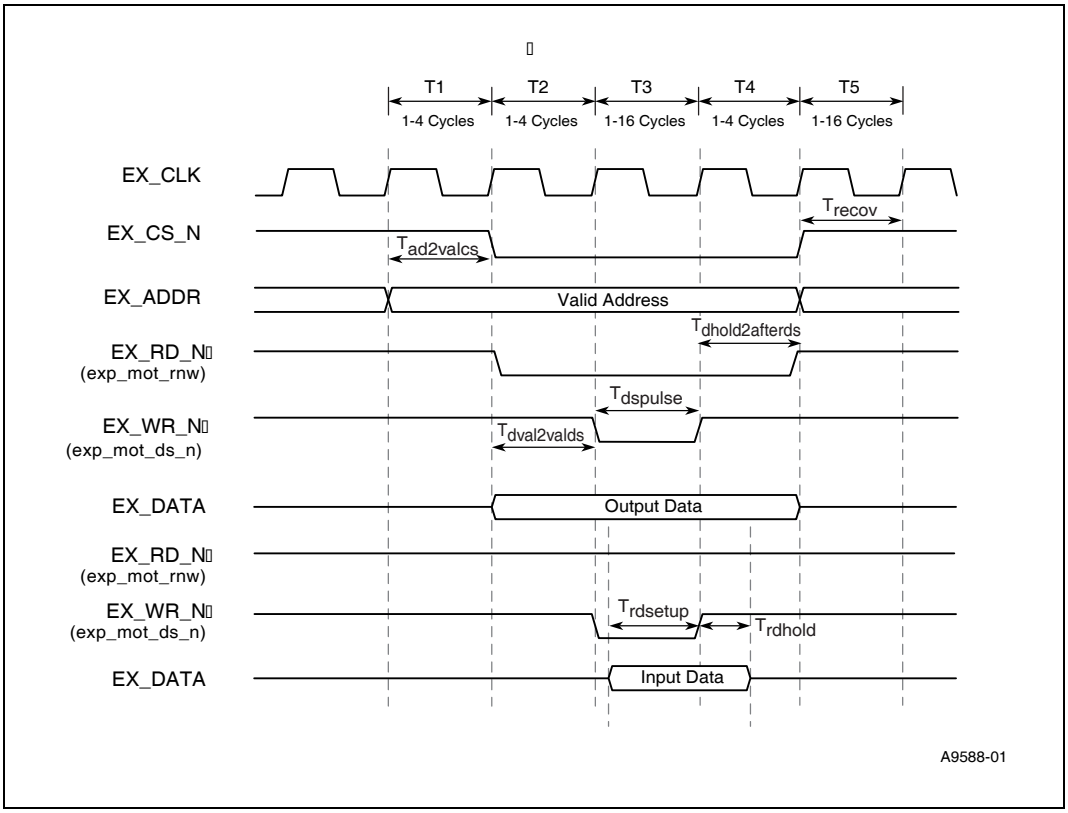


Table 65. Motorola* Simplex Mode Values (Sheet 1 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes
$T_{ad2valcs}$	Valid address to valid chip select	1	4	Cycles	1, 2, 7
$T_{dval2valds}$	Write data valid prior to EXP_MOT_DS_N falling edge	1	4	Cycles	3, 7
$T_{dspulse}$	Pulse width of the EXP_MOT_DS_N	1	16	Cycles	4, 7
$T_{dholdafterds}$	Valid data after the rising edge of EXP_MOT_DS_N	1	4	Cycles	5, 7

Note:
1. EX_ALE is not valid in simplex mode of operation.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration that the chip selects, address, and data (during a write) is held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in a synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Table 65. Motorola* Simplex Mode Values (Sheet 2 of 2)

Symbol	Parameter	Min.	Max.	Units	Notes
$T_{rdsetup}$	Data valid required before the rising edge of EXP_MOT_DS_N	14.7		ns	
T_{rdhold}	Data hold required after the rising edge of EXP_MOT_DS_N	2		ns	
T_{recov}	Time required between successive accesses on the expansion interface.	1	16	Cycles	6

Note:
1. EX_ALE is not valid in simplex mode of operation.
2. Setting the address phase parameter (T1) adjusts the duration that the address takes to appear to an external device.
3. Setting the data setup phase parameter (T2) adjusts the duration that the data takes to appear prior to a data strobe (read or write) to an external device.
4. Setting the data strobe phase parameter (T3) adjusts the duration that the data strobe takes to appear (read or write) to an external device. Data is available during this time as well.
5. Setting the data hold strobe phase parameter (T4) adjusts the duration that the chip selects, address, and data (during a write) is held.
6. Setting the recovery phase parameter (T5) adjusts the duration between successive accesses on the expansion interface.
7. T is the period of the clock measured in ns.
8. Clock to output delay for all signals is a maximum of 15 ns for devices requiring operation in a synchronous mode.
9. Timing was designed for system load between 5pF and 60pF for high drive settings

Table 66. Setup/Hold Timing Values in Asynchronous Mode of Operation

Parameter	Min.	Max.	Units	Notes
Output Valid after rising edge of EX_CLK		10	ns	1
Output Hold after rising edge of EX_CLK	0		ns	1
Input Setup prior to rising edge of EX_CLK	3.5		ns	1
Input Hold required after rising edge of EX_CLK	0.5		ns	1

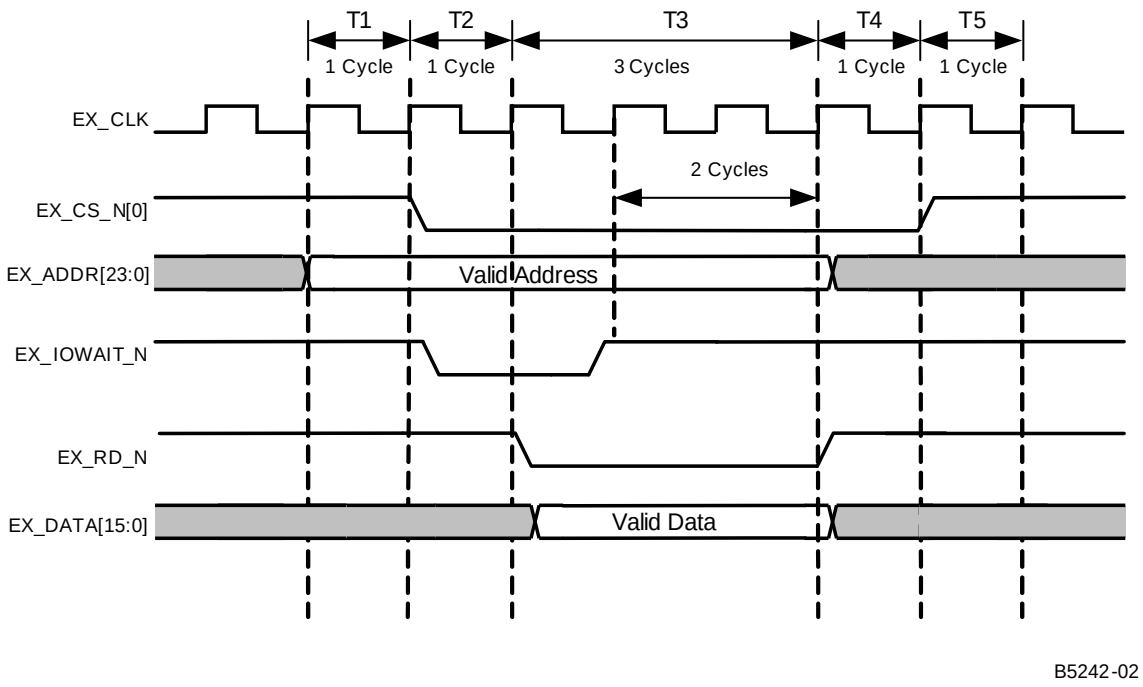
Note:
1. The Setup and Hold Timing values are for all modes.

5.7.2.7.3 EX_IOWAIT_N

The EX_IOWAIT_N signal is available for sharing by devices attached to chip selects 0 through 3, when configured in Intel or Motorola* modes of operation. The main purpose of this signal is to properly communicate with slower devices requiring more time to respond during data access. During idle cycles, the board is responsible for ensuring that EX_IOWAIT_N is pulled-up. The Expansion bus controller always ignores EX_IOWAIT_N for synchronous Intel mode writes.

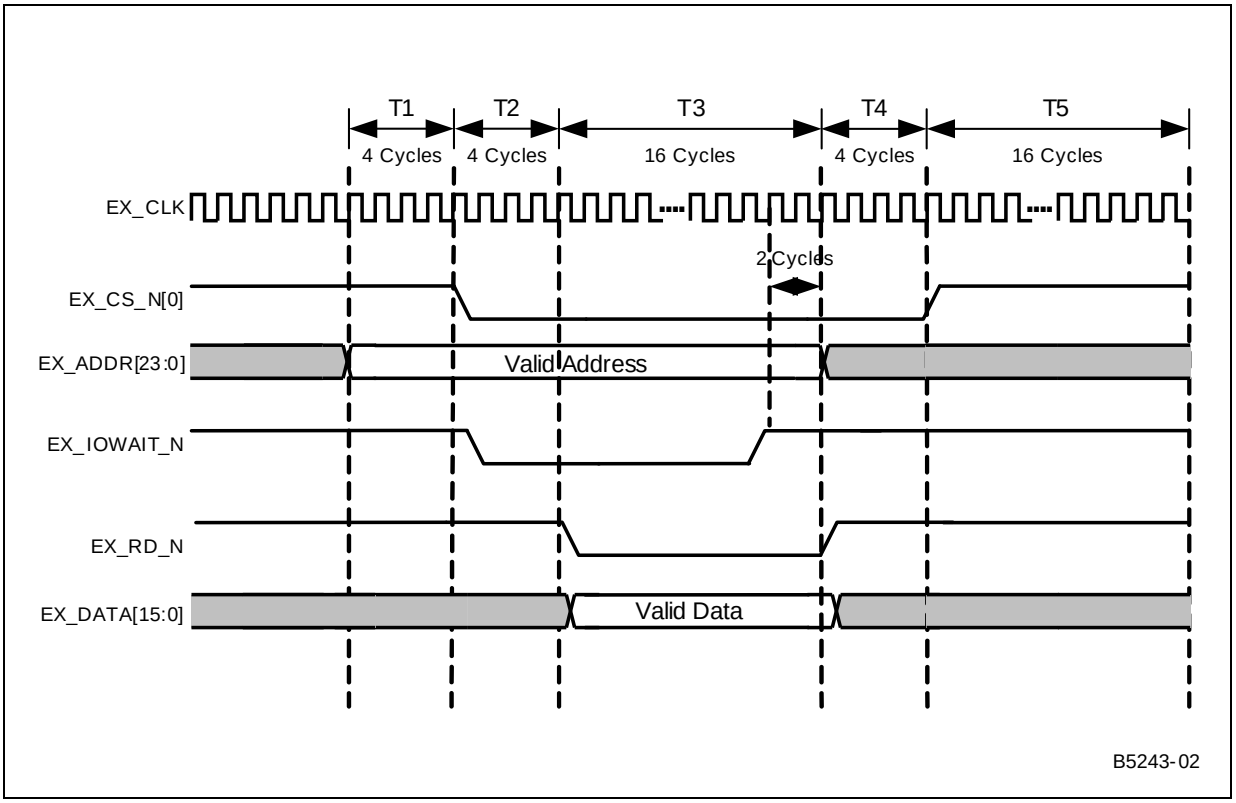
Refer to 'Using I/O Wait sub-section in the Expansion Bus Controller' chapter of the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for detailed information.

Figure 35. I/O Wait Normal Phase Timing



Note: Notice that the access is an Intel-style simplex read access. The data strobe phase is set to a value to last three clock cycles. The data is returned from the peripheral device prior to the three clocks and the peripheral device de-asserts EX_IOWAIT_N. The data strobe phase terminates after two clocks even though the strobe phase was configured to pulse for three clocks.

Figure 36. I/O Wait Extended Phase Timing



5.7.2.8 Serial Peripheral Port Interface Timing

Figure 37. Serial Peripheral Interface Timing

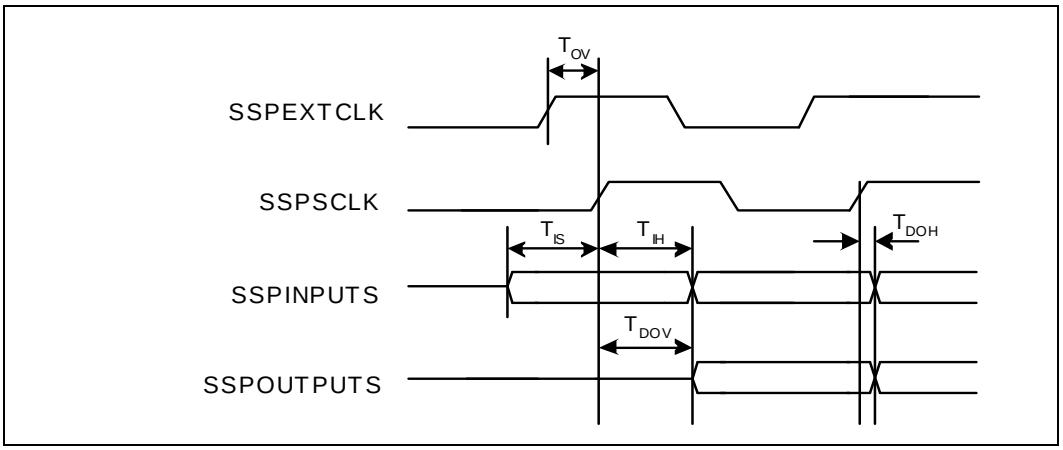


Table 67. Serial Peripheral Port Interface Timing Values

Symbol	Parameter	Min.	Max.	Units	Notes
T_{PER_INTCLK}	Minimum and maximum clock periods that can be produced by the SSP_SCLK when the clock is being generated from the internal 3.7033 MHz clock.	.00723	1.851	MHz	
T_{PER_EXTCLK}	Minimum and maximum clock period that can be produced by the SSP_SCLK when the clock is being generated from the externally supplied maximum clock rate of 33 MHz clock (SSP_EXTCLK).	.06445	16.5	MHz	
TOV	Output Valid Delay from SSP_EXTCLK to SSP_SCLK in an external clock mode	2	15	ns	
TIS	Input Setup time for data prior to the valid edge of SSP_SCLK. These signals include SSP_SRXD.	15		ns	
TIH	Input hold time for data after the to the valid edge of SSP_SCLK. These signals include SSP_SRXD.	0		ns	
TDOV	SSP_SCLK clock to output valid delay from output signals. These signals include SSP_STXD and SSP_SFRM.	1	6	ns	
TDOH	Output data hold valid from valid edge of SSP_SCLK. These signals include SSP_STXD and SSP_SFRM.	1		ns	

Note:
1. Clock jitter on the SSPSCLK is designed to be an average of the specified clock frequency. The SSPSCLK jitter specification is unspecified.

5.7.2.9 High-Speed, Serial Interface

Figure 38. High-Speed Serial Timings

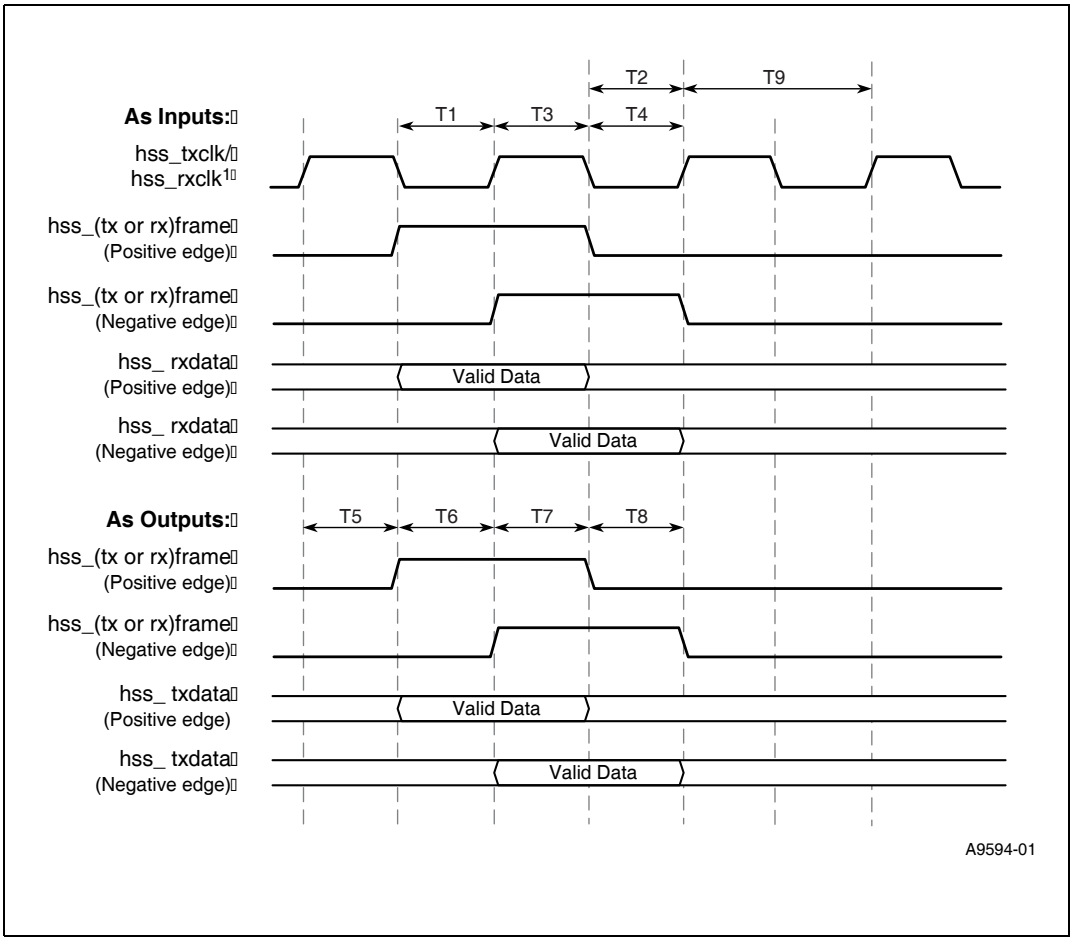


Table 68. High-Speed Serial Timing Values

Symbol	Parameter	Min.	Max.	Units	Notes
T1	Setup time of HSS_TXFRAME0, HSS_RXFRAME0, and HSS_RXDATA0 prior to the rising edge of clock	5		ns	1, 2, 3
T2	Hold time of HSS_TXFRAME0, HSS_RXFRAME0, and HSS_RXDATA0 after the rising edge of clock	0		ns	1, 2, 3
T3	Setup time of HSS_TXFRAME0, HSS_RXFRAME0, and HSS_RXDATA0 prior to the falling edge of clock	5		ns	1, 2, 3
T4	Hold time of HSS_TXFRAME0, HSS_RXFRAME0, and HSS_RXDATA0 after the falling edge of clock	0		ns	1, 2, 3
T5	Rising edge of clock to output delay for HSS_TXFRAME0, HSS_RXFRAME0, and HSS_TXDATA0		15	ns	1, 4
T6	Falling edge of clock to output delay for HSS_TXFRAME0, HSS_RXFRAME0, and HSS_TXDATA0		15	ns	1, 3, 4
T7	Output Hold Delay after rising edge of final clock for HSS_TXFRAME0, HSS_RXFRAME0, and HSS_TXDATA0	0		ns	1, 3, 4
T8	Output Hold Delay after falling edge of final clock for HSS_TXFRAME0, HSS_RXFRAME0, and HSS_TXDATA0	0		ns	1, 3, 4
T9	HSS_TXCLK0 period and HSS_RXCLK0 period	1/8.192 MHz	1/512 KHz	ns	5

Notes:

1. HSS_TXCLK0 and HSS_RXCLK0 can come from external independent sources or driven by the IXP43X network processors. The signals are shown to be synchronous for illustrative purposes and are not required to be synchronous.
2. Applicable when the HSS_RXFRAME0 and HSS_TXFRAME0 signals are being driven by an external source as inputs into the IXP43X network processors. Always applicable to HSS_RXDATA0.
3. The HSS_RXFRAME00 and HSS_TXFRAME0 can be configured to accept data on the rising or falling edge of the given reference clock. HSS_RXFRAME0 and HSS_RXDATA0 signals are synchronous to HSS_RXCLK0 and HSS_TXFRAME0 and HSS_TXDATA0 signals are synchronous to the HSS_TXCLK0.
4. Applicable when the HSS_RXFRAME0 and HSS_TXFRAME0 signals are being driven by the IXP43X network processors to an external source. Always applicable to HSS_TXDATA0.
5. The HSS_TXCLK0 can be configured to be driven by an external source or be driven by the IXP43X network processors. The slowest clock speed that can be accepted or driven is 512 KHz. The maximum clock speed that can be accepted or driven is 8.192 MHz. The clock duty cycle accepted is 50/50 + 20%.
6. Timing was designed for system load between 5 pF and 30 pF for high drive setting

5.7.2.10 JTAG

Figure 39. Boundary-Scan General Timings

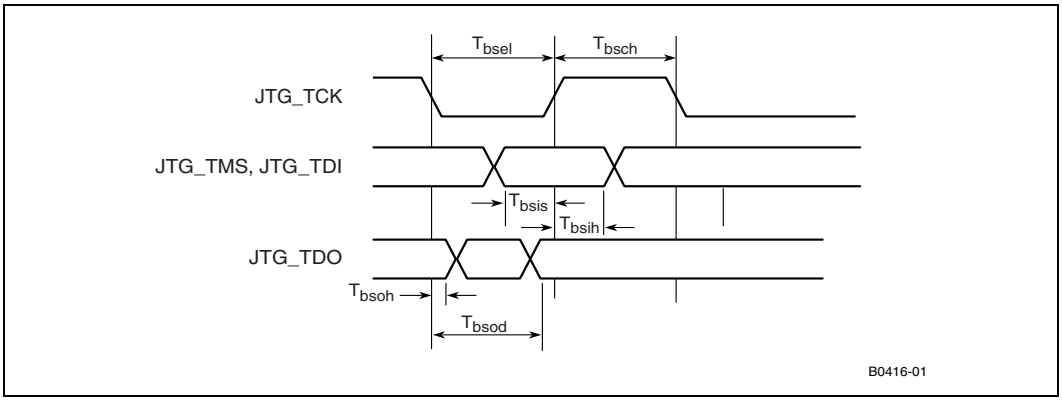


Figure 40. Boundary-Scan Reset Timings

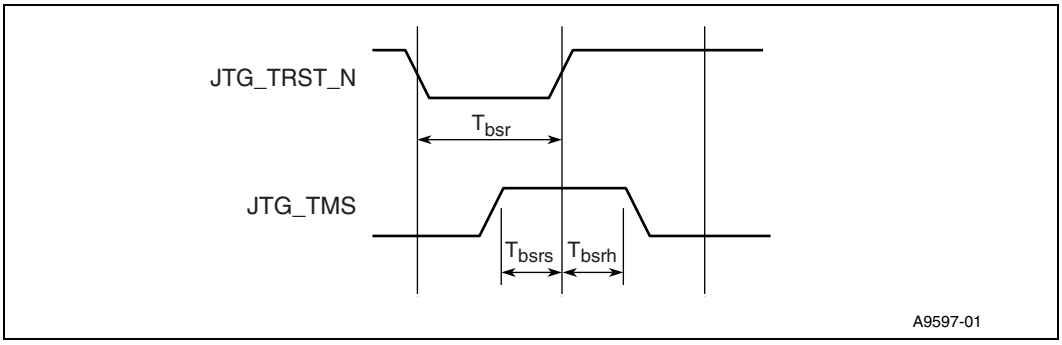


Table 69. Boundary-Scan Interface Timings Values

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTG_TCK low time		50			ns	2
T_{bsch}	JTG_TCK high time		50			ns	2
T_{bsis}	JTG_TDI, JTG_TMS setup time to rising edge of JTG_TCK		10			ns	
T_{bsih}	JTG_TDI, JTG_TMS hold time from rising edge of JTG_TCK		10			ns	
T_{bsoh}	JTG_TDO hold time after falling edge of JTG_TCK		1.5			ns	1
T_{bsod}	JTG_TDO clock to output from falling edge of JTG_TCK				40	ns	1
T_{bsr}	JTG_TRST_N reset period		30			ns	
T_{bsrs}	JTG_TMS setup time to rising edge of JTG_TRST_N		10			ns	
T_{bsrh}	JTG_TMS hold time from rising edge of JTG_TRST_N		10			ns	

Note:
1. Tests are completed with a 40-pF load to ground on JTAG_TDO.
2. JTG_TCK can be stopped indefinitely either in the low or high phase.

5.7.3 Reset

The IXP43X network processors can be reset in any of the following three modes:

- Cold Reset
- Warm Reset
- Soft Reset

Normally, a Cold Reset is executed each time power is initially applied to the board, a Warm Reset is executed when it is only intended to reset the IXP43X network processors, and a Soft Reset is executed by the watchdog timer.

5.7.3.1 Cold Reset

A Cold Reset condition is when the network processor is initially powered-up and has successfully come out of the Reset. During this state all internal modules and registers are set to the initial default state. To successfully come out of reset, two things must occur:

- Proper power sequence as described in Section 5.8, “Power Sequence” on page 125

- Followed by proper resetting of PWRON_RST_N and RESET_IN_N signals as described in Section 5.7.3.4, “Reset Timings” on page 124

The following procedural sequence must be followed to achieve a successful cold reset:

1. VCC and VCC33 power supplies must reach steady state
2. Hold PWRON_RST_N and RESET_IN_N asserted for 2000nSec
3. De-assert PWRON_RST_N (signal goes high with the help of a pull-up resistor)
4. Continue to hold RESET_IN_N asserted for at least 10nSec more after releasing PWRON_RST_N
5. De-assert RESET_IN_N (signal goes high with the help of a pull-up resistor)
6. The network processor asserts PLL_LOCK indicating that the processor has successfully come out of Reset

5.7.3.2 Hardware Warm Reset

A Hardware Warm Reset can only be asserted when PWRON_RST_N is de-asserted and the network processor is in a normal operating mode. A Hardware Warm Reset is initiated by the assertion of RESET_IN_N. During this state, all internal registers and modules are set to their initial default state except for the PLL internal modules. Since the PLL modules are not reset, the Reset sequence is executed much faster by the processor.

The following procedural sequence must be followed to achieve a successful warm reset:

1. The system must have previously completed a Cold Reset successfully.
2. PWRON_RST_N must be de-asserted (held high for the entire process).
3. Hold RESET_IN_N asserted for 500nSec.
4. De-assert RESET_IN_N (signal goes high with the help of a pull-up resistor)
5. The network processor asserts PLL_LOCK indicating that the processor has successfully come out of reset.

5.7.3.3 Soft Reset

A Soft Reset condition is accomplished by the usage of the hardware Watch-Dog Timer module, and software to manage and perform counter updates. For a complete description of Watch-Dog Timer functionality, refer to Watchdog Timer Operation sub-section in the Operating System Timer Chapter of the *Intel® IXP43X Product Line of Network Processors Developer’s Manual*.

The Soft Reset is similar to what is described in Section 5.7.3.2. The main difference is that there is no hardware requirement; everything is done within the network processor and software support. That is why it is also referred to as a Soft Warm Reset. Since Hardware Warm Reset and Soft Warm Reset are very similar, there must be a way to determine which reset was last executed after recovering. This is done by reading the Timer Status Register bit 4 (Warm Reset). If this bit was last set to 1, it will indicate that a Soft Reset was executed, and if the bit was last reset to 0, then it will indicate that the processor has just come out of either a Hardware Warm Reset or a Cold Reset.

5.7.3.4 Reset Timings

Figure 41. Reset Timings

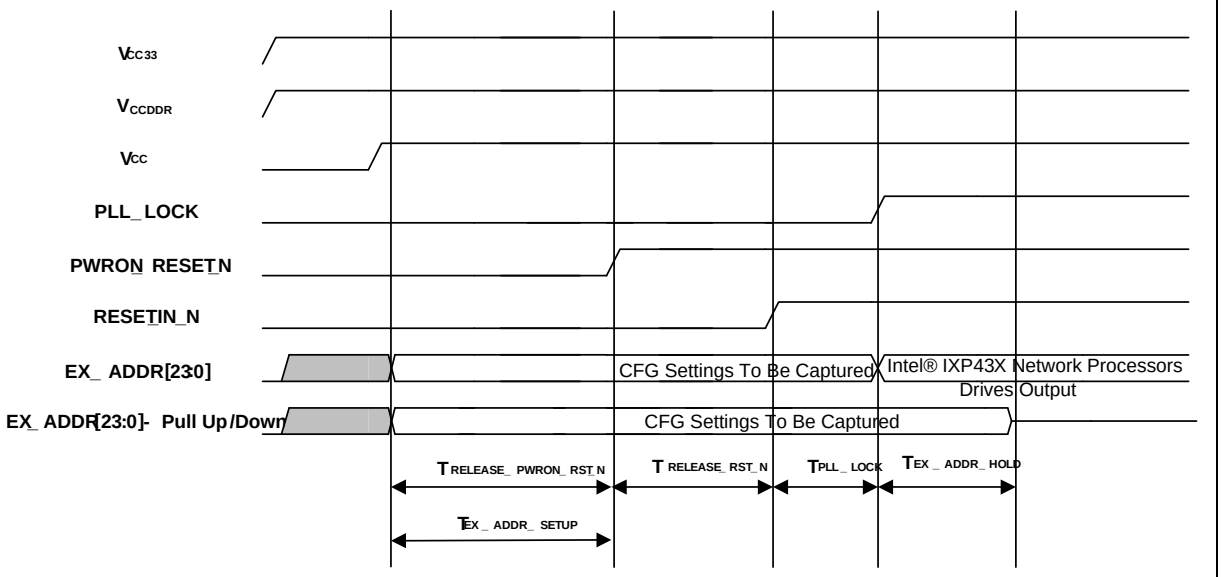


Table 70. Reset Timings Table Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Note
$T_{RELEASE\_PWRON\_RST\_N}$	Minimum time required to hold the PWRON_RST_N at logic 0 state after stable power has been applied to the IXP43X network processors while using a crystal to drive the processor's system clock. (OSC_IN and OSC_OUT)	500			ms	1
$T_{RELEASE\_RESET\_IN\_N}$	Minimum time required to hold the RESET_IN_N at logic 0 state after PWRON_RST_N has been released to a logic 1 state. The RESET_IN_N signal to be held low when the PWRON_RST_N signal is held low.	10			ns	
T_{PLL_LOCK}	Maximum time for PLL_LOCK signal to drive to logic 1 after RESET_IN_N is driven to logic 1 state. The boot sequence does not occur until this period is complete.	720		1500	ns	
$T_{EX\_ADDR\_SETUP}$	Minimum time for the EX_ADDR signals to drive the inputs prior to RESET_IN_N being driven to logic 1 state. This is used for sampling configuration information.	50			ns	2
$T_{EX\_ADDR\_HOLD}$	Minimum/maximum time for the EX_ADDR signals to drive the inputs prior to PLL_LOCK being driven to logic 1 state. This is used for sampling configuration information.	0		20	ns	2
T_{WARM_RESET}	Minimum time required to hold RESET_IN_N signal at logic 0 to cause a warm reset in the IXP43X network processors. The power must remain stable and the PWRON_RST_N signal must remain stable (logic high) during the process.	500			ns	

Note:
1. $T_{RELEASE\_PWRON\_RST\_N}$ is the time required for internal oscillator to reach stability. When an external oscillator is used instead of a crystal, the delay required is 2000-ns instead of 500-ms.
2. The expansion bus address is captured as a derivative of the RESET_IN_N signal going high. When a programmable-logic device is used to drive the EX_ADDR signals instead of pull-downs, the signals should be active till PLL_LOCK is active.

5.8 Power Sequence

The 3.3-V I/O voltage (V_{CC33}) and the 2.5/1.8-V I/O voltage (V_{CCDDR}) is powered up at least 1 µs before the core voltage (V_{CC}). The core voltage (V_{CC}) of the IXP43X network processors must not become stable prior to 3.3-V I/O voltage (V_{CC33}) or the 2.5/1.8-V I/O voltage (V_{CCDDR}).

Sequencing between V_{CC33} and V_{CCDDR} can occur in any order with respect to one another. T_{IO_PHASE} can be:

- V_{CC33} prior to V_{CCDDR}
- V_{CCDDR} prior to V_{CC33}
- V_{CC33} simultaneously to V_{CCDDR}

Note: During the interval between V_{CCDDR} and V_{CC} ramps, the DDR pin states will be held to V_{ss}.

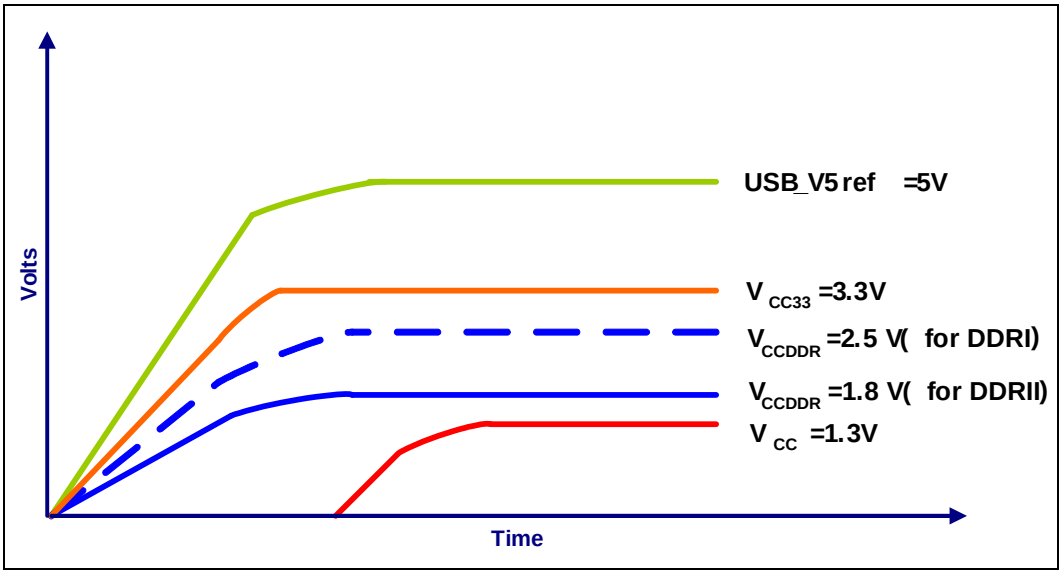
The $V_{USBAUPLL}$, $V_{USBCORE}$, and V_{CCA} voltage (1.3V) follow the V_{CC} voltage power-up pattern. The V_{CCP_OSC}, V_{CCPUSB}, and V_{CCAUBG} voltage (3.3V) follows the V_{CC33} voltage power-up pattern.

The value for T_{POWER_UP} to be at least 1 µs after the later of V_{CC33} and V_{CCDDR} reaches stable power. The T_{POWER_UP} timing parameter is measured between the later of the I/O power rails (V_{CC33} at 3.3 V or V_{CCDDR} at 2.5/1.8 V) and V_{CC} at 1.3 V.

The USB ports in the IXP43X network processors have a special requirement on power up sequence if the USB_V5ref is connected to a 5V power supply. The USB_V5ref ports to be powered up are as follows:

- USB_V5ref prior to V_{CC33}
- If USB_V5ref is powered up simultaneously to V_{CC33}, Voltage level at pin USB_V5ref must be equal to or higher than V_{CC33} all the time.

Figure 42. Power-up Sequence Timing



The following power assessments assume full-speed operation by all peripherals and internal components. If applications do not require usage of certain peripherals or full-speed operation from all the peripherals are not required, the power required by the part can be significantly less than the numbers stated in the following table.

5.9 Power Dissipation

Table 71. Power Dissipation Values

Part Type	Power Rail	I_{CC_TOTAL} (mA)	Power Per Rail (mW)†	Typical Power Dissipation (Watts)
Intel® IXP43X Product Line of Network Processors — 400 MHz	3.3 V	310	1022	3.04 (2.64)
	2.5 V (1.8 V)	260 (138)	649 (249)	
	1.3 V	1051	1366	
Intel® IXP43X Product Line of Network Processors — 533 MHz	3.3 V	310	1023	3.08 (2.68)
	2.5 V (1.8 V)	259 (138)	648 (249)	
	1.3 V	1081	1406	
Intel® IXP43X Product Line of Network Processors — 667 MHz	3.3 V	311	1027	3.13 (2.73)
	2.5 V (1.8 V)	258 (138)	644 (249)	
	1.3 V	1119	1455	
† Power in mW is calculated using Typical Vcc specification for each power rail. †† Power Dissipation (Watts) figures are for DDR-I (2.5V) and DDR-II (1.8V) respectively.				

5.10 Ordering Information

Contact your local Intel sales representative for ordering information.

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